JUST ANOTHER FABLESS STARTUP ?

GRAPHCORE

JUST ANOTHER FABLESS STARTUP MAKING A CHIP USING STANDARD PROCESSES AT TSMC AND ASE...?

Not quite. AI chips that go into server farms in amongst huge GPUs, CPUs and network processors have engineering challenges that established companies might have already solved, but the solutions are not necessarily well known across the industry. This leads to a lot of discovery-led engineering problem solving. I will describe some of these, focussing especially on those that arise in the area of test.

Over the past 20 years, **Paul Freeman** has created and managed silicon chip manufacturing processes for three VC-funded Fabless Semiconductor startup companies (Element 14, Icera and Graphcore), from nothing to high volume success, resulting in over $1B of exit value and the shipment of tens of millions of units.

Paul Elford is currently in charge of Production Test Outsourcing in Graphcore, working on the next generation of AI processors.

He has over 25 year experience in Semiconductor Product and Test Engineering roles. Starting as a Product Engineer in GEC Plessey he has worked for a variety of companies from raw start-ups to establish multi-nationals; including Directing the Product and Test Dept of the Semtech LoRa IoT Product line.

WHAT WE DO…

Colossus:

- 1280x 100GFlop Processors with 256K Memory on a single die
  - >50Billion Logic Transistors
  - ~2.6Billion Memory Bits
- Exchange block to allow any processor to communicate with any other processor
- 12x 8Gbps SERDES ports to allow any processor to communicate off-chip with any other processor in a system

Wafer:

- 25 x 32mm Die Size
- 66 Die per wafer
- 27K+ Bumps per Die
- 7K+ needle Probe Card

Package

- 47.5 x 47.5 mm Package
- 2116 Pin Socket
- +250 integrated caps
- Metal stiffener ring
- Exposed silicon

… AND THE CHALLENGES WE FACE

Many challenges are not plannable.

- We are combining technologies in a way that e.g. AMD, Intel, NVidia have already done and understand and have built up an appropriate knowledge base.

We utilise very advanced technology suppliers (e.g. Salland, ASE, TSMC, Teradyne, etc.)

- But they do not need to see and share the full picture: we have to do that.
- We have to discover for ourselves by orchestrating activity across our suppliers.

Challenges are rarely one dimensional, e.g.

- Vdd-to-Vss shorts: Tester? Test Hardware? Silicon? Packaging? Assembly? Materials?

Many challenges are new and (almost) unique:

- e.g. “test at high voltage” sounds easy, however…
- High Vdd = High Idd = High Heat = Higher Idd = meltdown
- Therefore difficult to implement in practice, and needs characterisation of device and environment

TEST ENG ROLE

First Silicon

- Efficient first-silicon bring-up needs between 10 and 20 chip testers.
- These typically cost $1M each, but after the first 2 weeks we might only need 3 or 4.

Low cost Bench testers developed based on Tessent (OpelKelly) boards

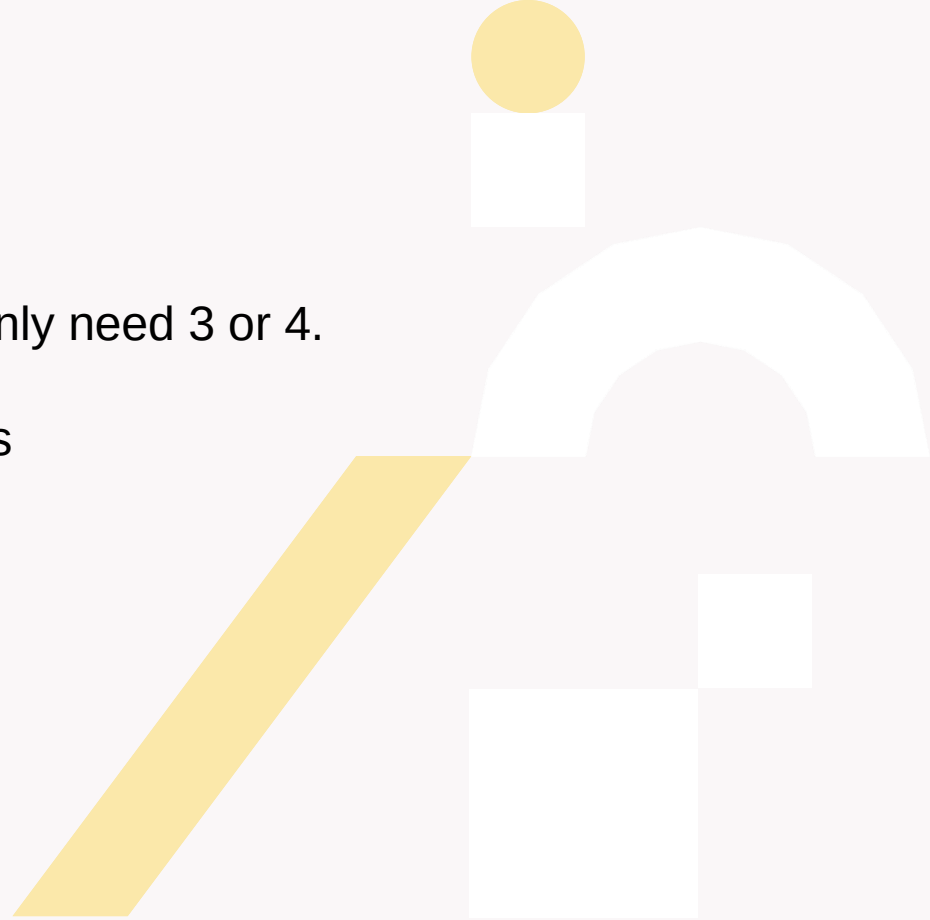
- Allows Functional and Scan Test access
- Allows link to Design simulation environment for bring-up debug
- Allows debug of most ATE test patterns
- Flexible and reusable
- ATE agnostic

Production ATE HW and SW development in Salland

- ATE plus support equipment
- ATE Knowledge

Test Eng becomes

- Debug and validation on custom test equipment
- Bridge between DFT and subcon
- Outsourcing Management
- Production Offload



(A) LOT-ON-A-CHIP

66 Die Per Wafer : 1280 Processors per Chip : 84480 per wafer

- Equivalent to running a Production Lot on one Chip
- Yield is not the same as Defectivity:
  - 1 Die = 1.5%, 1 Processor = 0.000011%
- Redundancy means “some” of these many be Faulty, but DUT is still Bin 1

Data Management

- 1280 Processor tested with 5 tests at 3 VDD levels = +19K Test Results.
- Test Program becomes Data Management program
- Data Analysis must treat each die as multiple devices
- 66 Die per wafer becomes

Device Parametric performance

- How does parametric performance vary across the die?

Power Management

- Test Time = f(Power)
- Test at high Vdd / Idd requires clear understanding of thermal characteristics

Fault Detection / Reliability

- A 1-in-2-billion failure rate causes almost every chip to contain a fault.
- Manufacturing test can cause faults to be repaired but what remains is a reliability hazard.