



Testing AI Devices Challenges and Trends

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```
...mirror_mod.mirror_object = ...
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mirror_mod.use_x = True
mirror_mod.use_y = False
mirror_mod.use_z = False
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...selection at the end -add ...
..._ob.select= 1
..._ob.select=1
context.scene.objects.active
["Selected" + str(modifier_...
..._ob.select = 0
..._context.selected_ob
...please select ex...
```

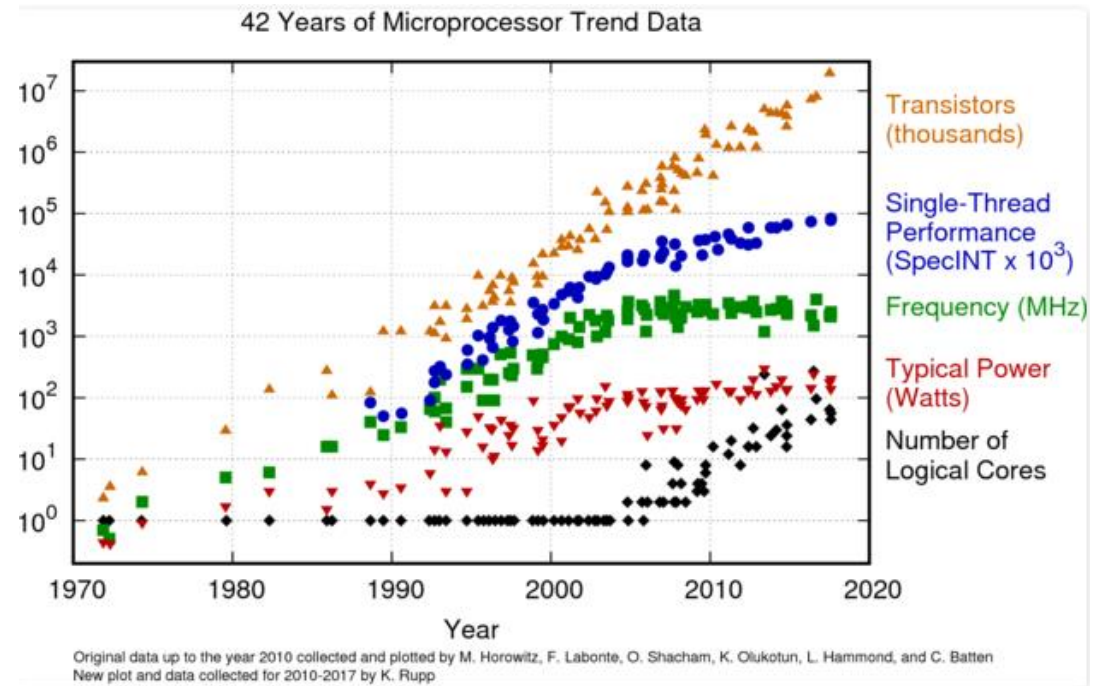
Technology Trends 2019+

Moore's Law continuing



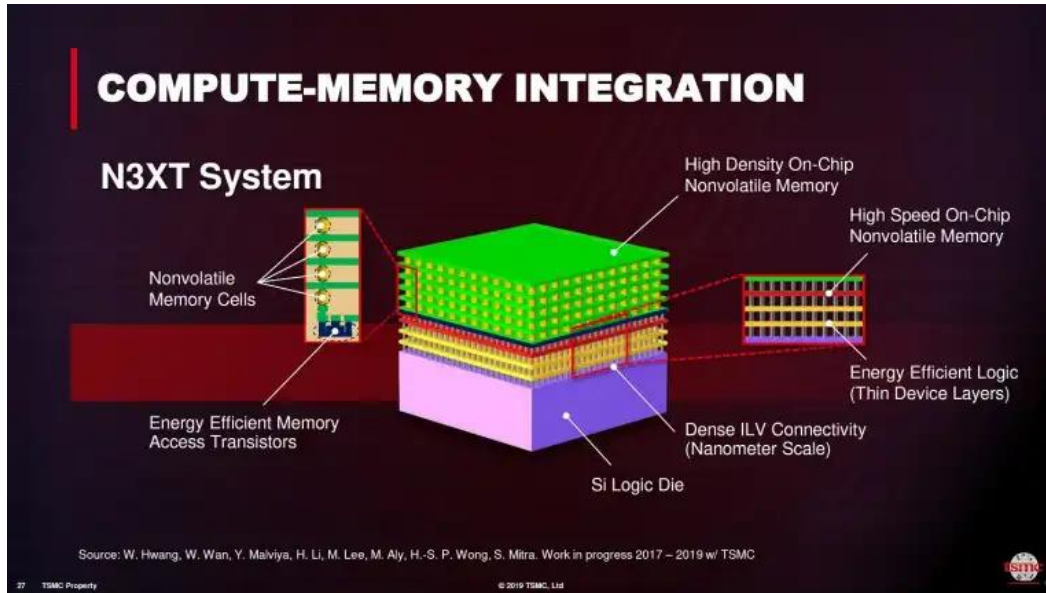
Source: HotChips 2019 - Philip Wong CTO

- 7nm → 5nm → 3nm **Roadmap on Track**
- Transistor density scaling on track **until 2050**



- Major performance growth through **parallelization**
- **3D structures** required
- **Advanced packaging** becomes a technology driver

3D Packaging

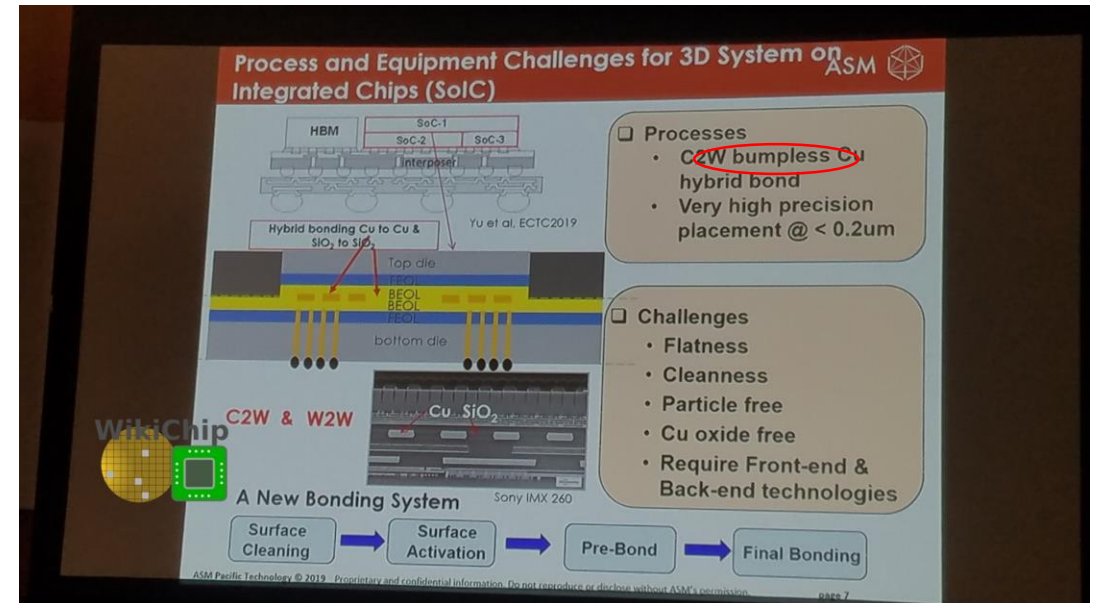


Courtesy of TSMC - SemiWest 2019

- 3D System on Integrated Chips (e.g. **SoIC**)
 - SoIC enables e.g. **chip-partitioning** of logic and cache memory like SRAM

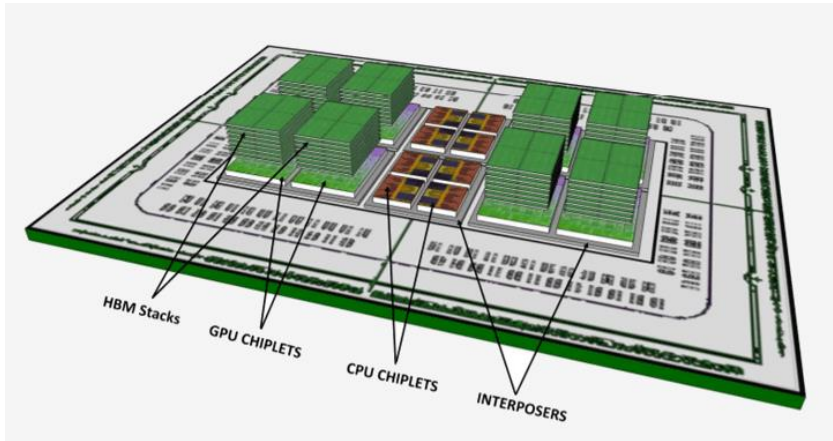
HPC/AI

- **Memory Wall** → Most energy for data transfer
- **On-chip caches** → ~4G at 1.4nm node
- **HBM**
- **Chiplets + 3D stacked memory** for fast data transfer

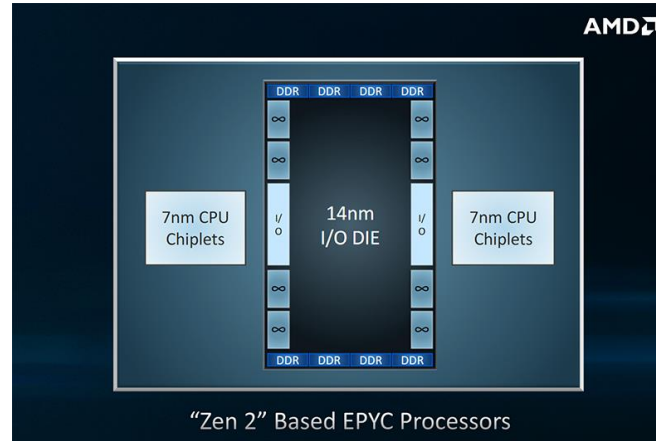


Courtesy of ASM

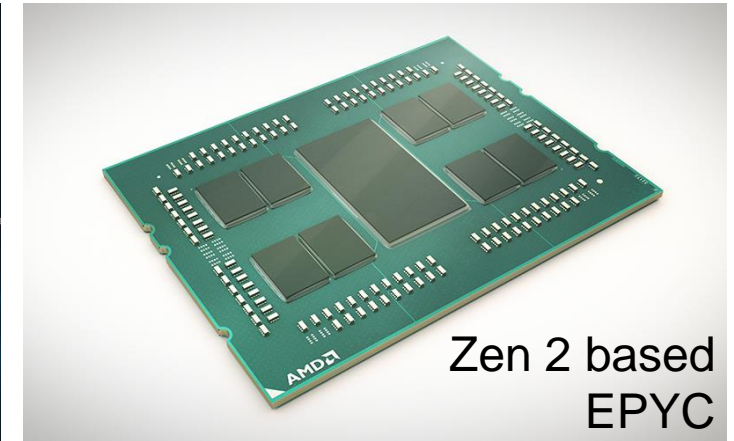
Chiplets



Courtesy of Intel



Courtesy of AMD



Courtesy of AMD

- “Opportunity to become **less node-dependent**” – Philip Wong TSMC
- **CP test coverage** is critical
- **System test coverage** at FT and CP



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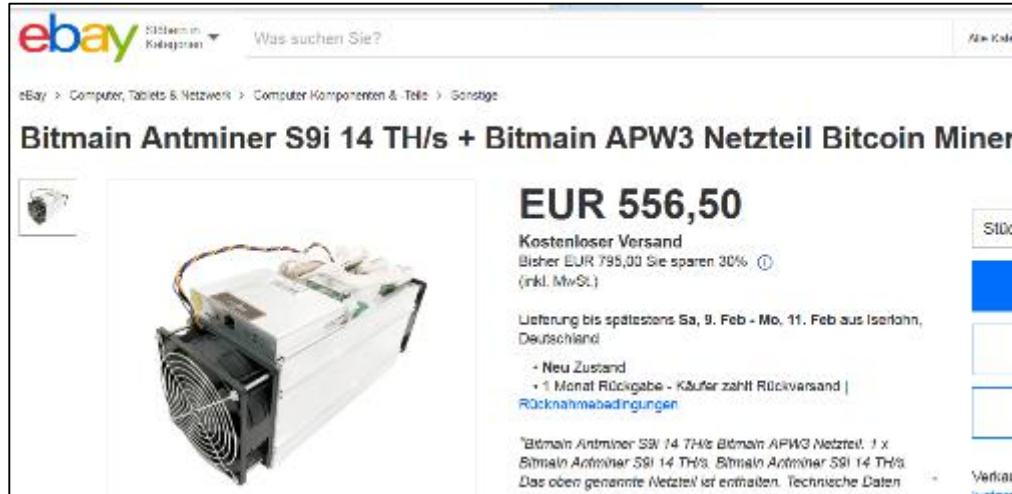
#selection at the end -add
mirror_ob.select= 1
obj_ob.select=1
context.scene.objects.active = obj_ob
print("Selected" + str(modifier_ob))
mirror_ob.select = 0
bpy.context.selected_objects = [obj_ob]
print("please select obj")

OPERATOR CLASSES
```

AI Device Trends

AI / (High) Performance Compute Landscape

Cryptocurrencies



Server Farms



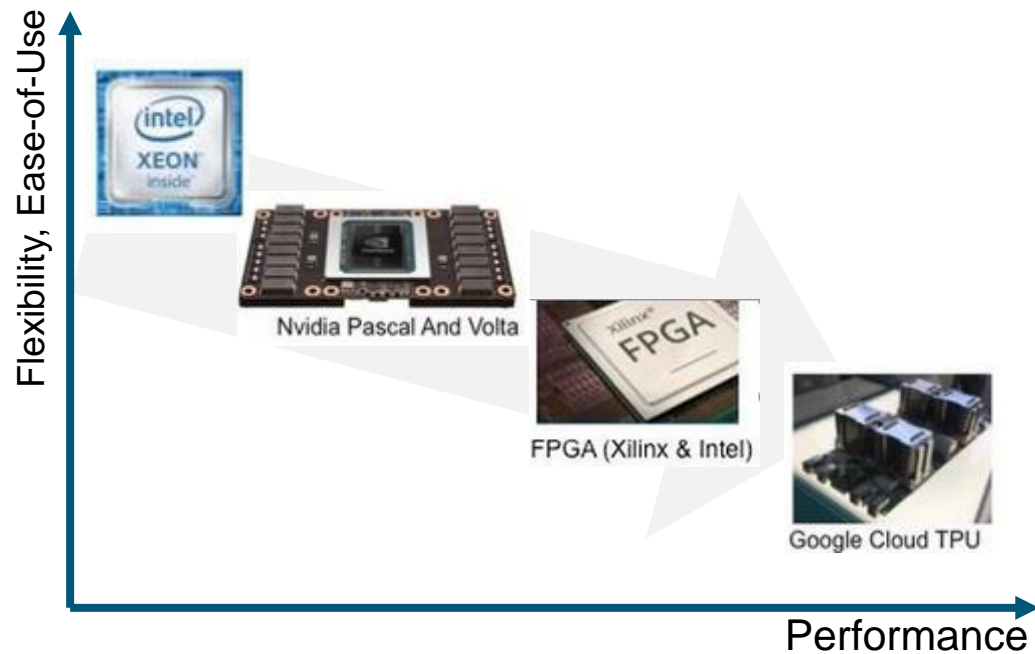
Edge Computing

Autonomous Cars



AI Trends

AI is moving from general purpose to custom



System Companies

- Tech industries biggest companies bring chip design in-house
- **Drivers:** cost, risk mitigation, better SW integration, differentiation

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Alibaba.com™



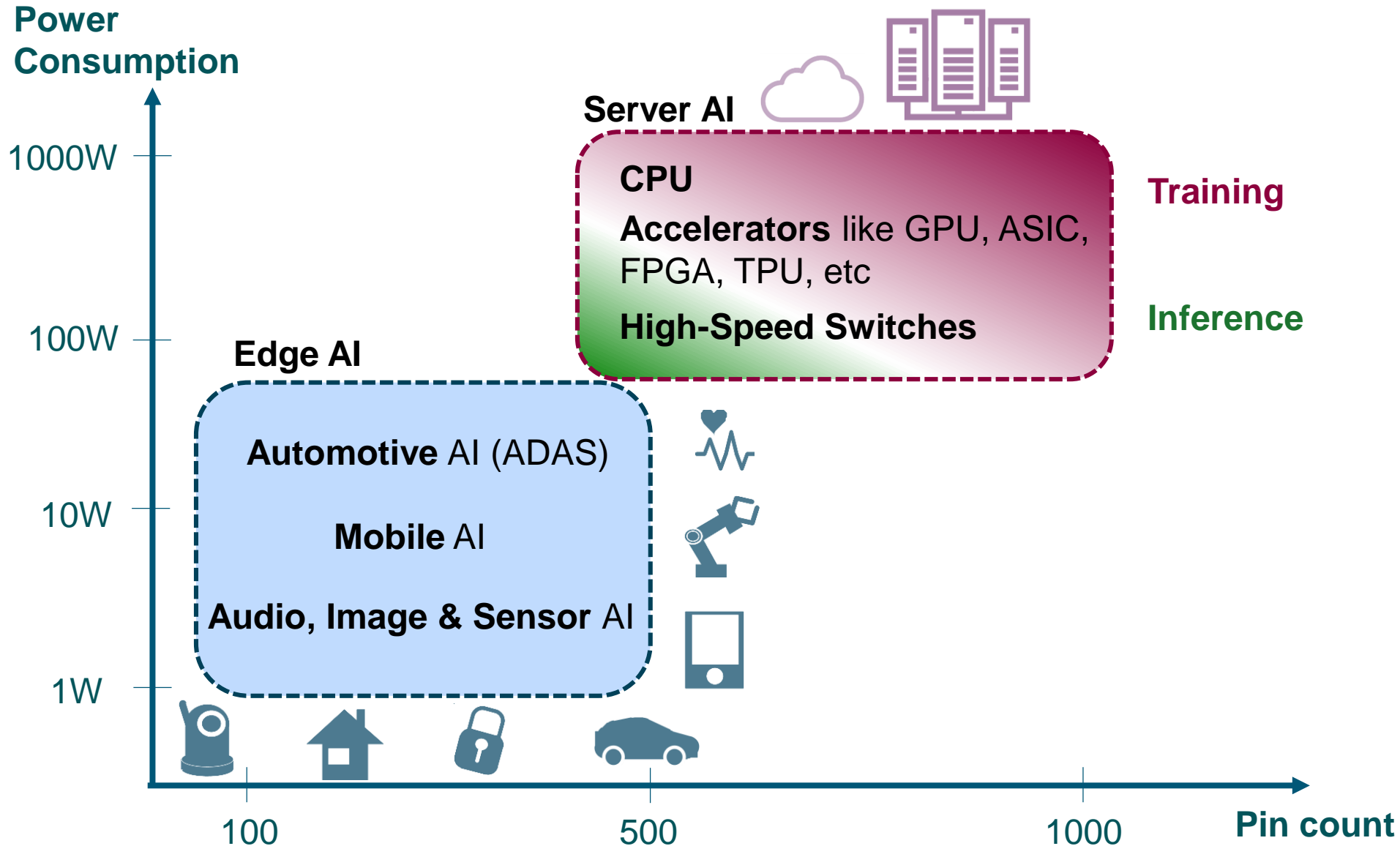
amazon

Baidu 百度

Microsoft

Google

AI Market Segmentation



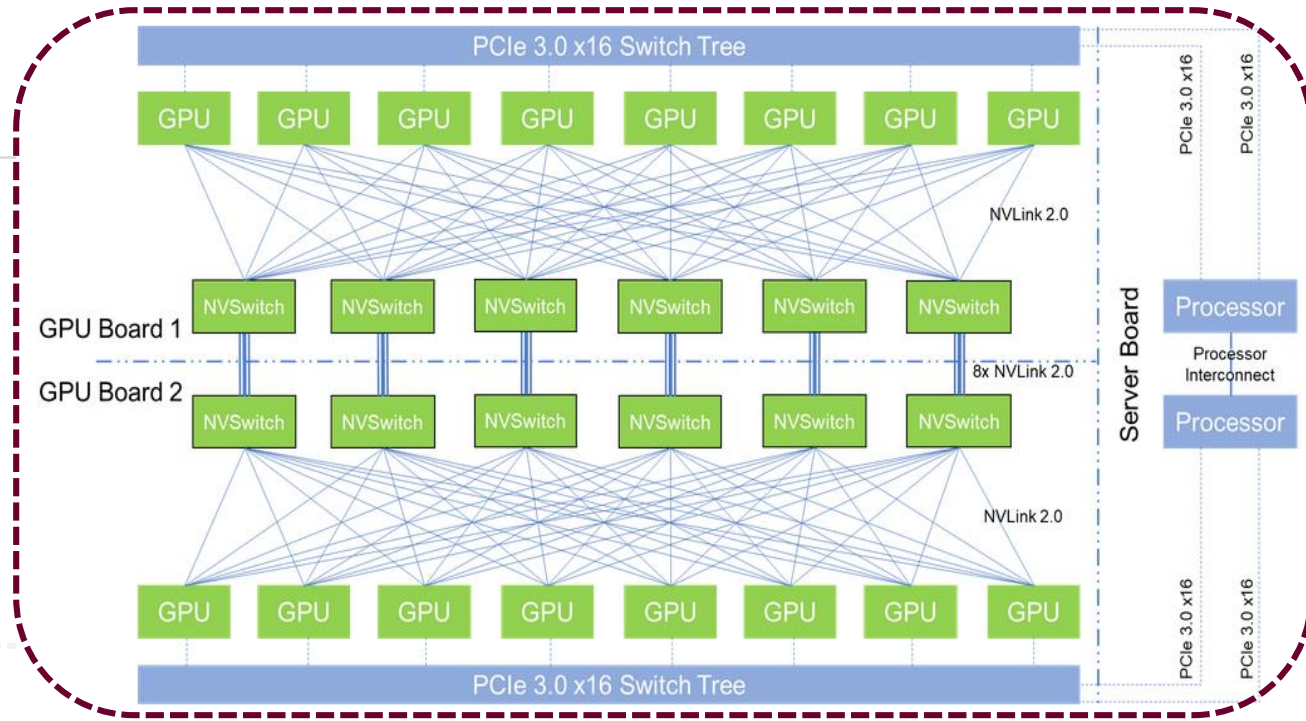
AI Market Segmentation

Power Consumption



Server AI

Examples:
AMD CPU Rome
nVidia GPU Tesla
NVLink Switch Willow



Edge AI

enable real time actions

Image AI

(surveillance, expression, robots, drones)

→ e.g. Jetson Edge AI

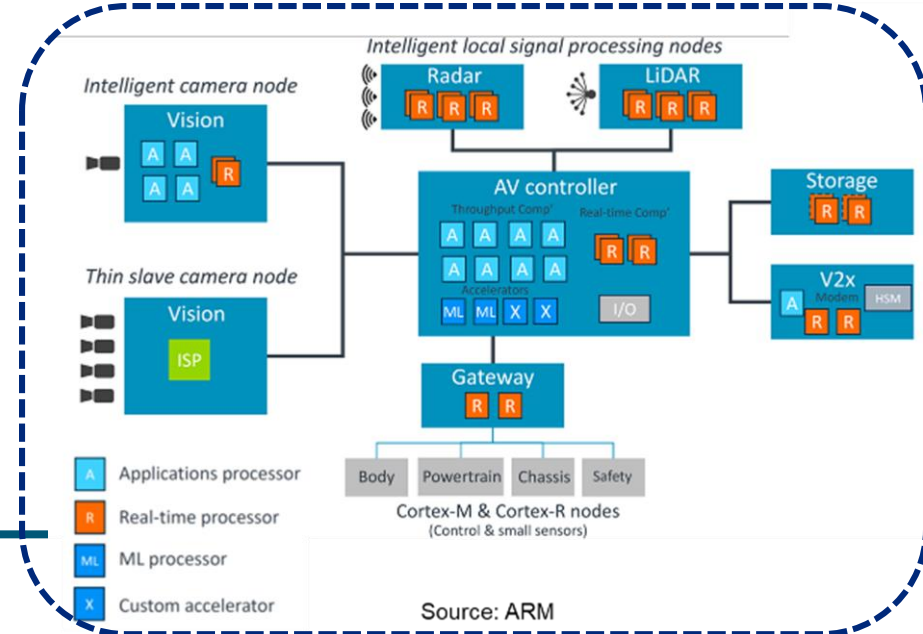
Audio AI

(noise reduction, audio/write/ctrl)

→ RF & Analog might be integrated

Sensor AI

(machine state, body monitoring)



Automotive AI is like Edge AI, but:

- more power
- high performance
- highest quality, 0 DPPM

Pin count



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Testing Challenges

V93000 – Leader in HPC/AI Test → Since 1999

Key Testing Challenges for 7nm+, 5nm, 3nm ...

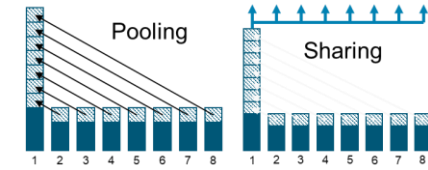
COST

DPPM

Fundamental Testing Challenges

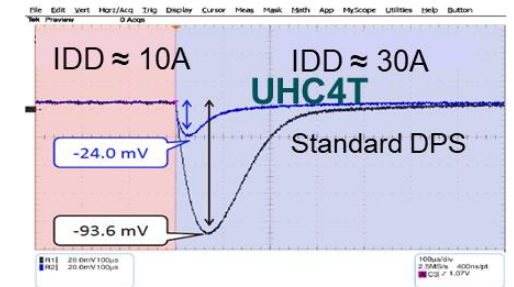
1. New technologies & higher complexity drive deeper scan

- License free **pooling** and **fan-out** technology, unlimited **speed**
- **Largest Scan** per pin



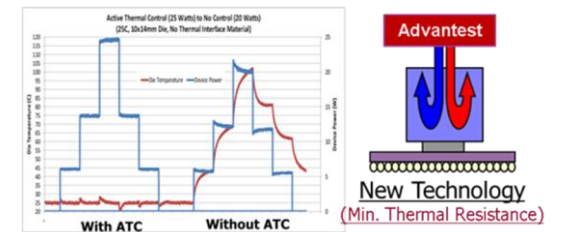
2. Superior mix of DPS instruments

- Simple configurations w/ **two types**: high-density vs high-power
- Best in class **step response** for **1000A** and more → yield
- Large **installed base** at OSATs to lower CoT



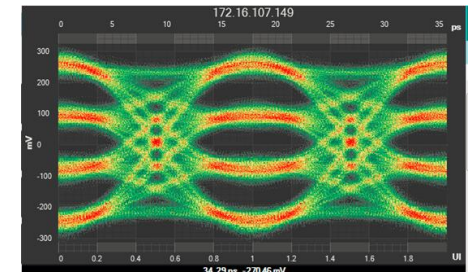
3. Test cell with active thermal control

- For accurate, fast & stable measurements → **best in class ATC** Test cell temperature trigger tool incl. patented **smart pre-trigger**



4. High-speed Instruments

- Need to cover next gen HSIO interfaces 112G PAM4.



Tester Requirements for Different AI Segments

1. Edge AI

- Scalable platform to start from low-end Edge AI
- Attractive CoT → optimized VM usage (save up to 80% VM)



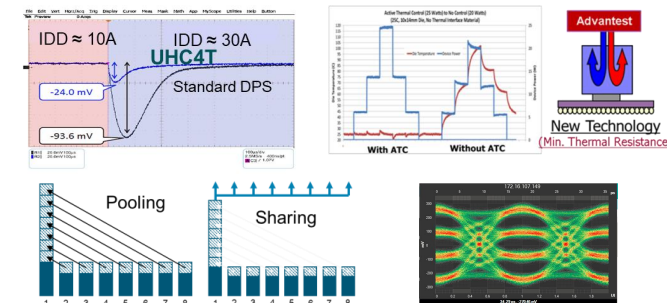
2. Automotive AI

- Scalable platform to span from low-end to high-end
- Attractive CoT → optimized VM usage (save up to 80% VM)
- One stop shopping incl handler/ATC and SLT (DPPM & CoT)

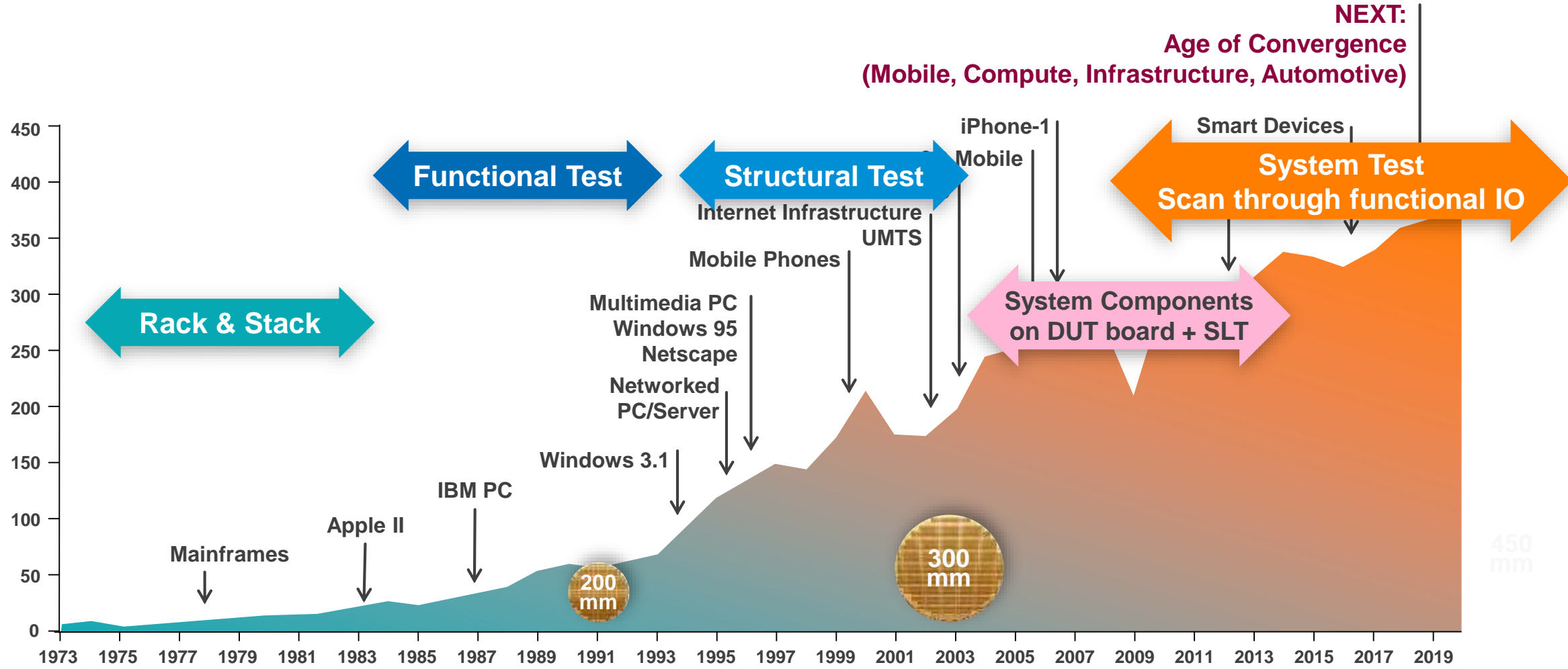


3. Server AI

- All fundamental performance compute test requirements
- Future proven



Paradigm Shifts in ATE



Cost + DPPM Reduction across Workflow

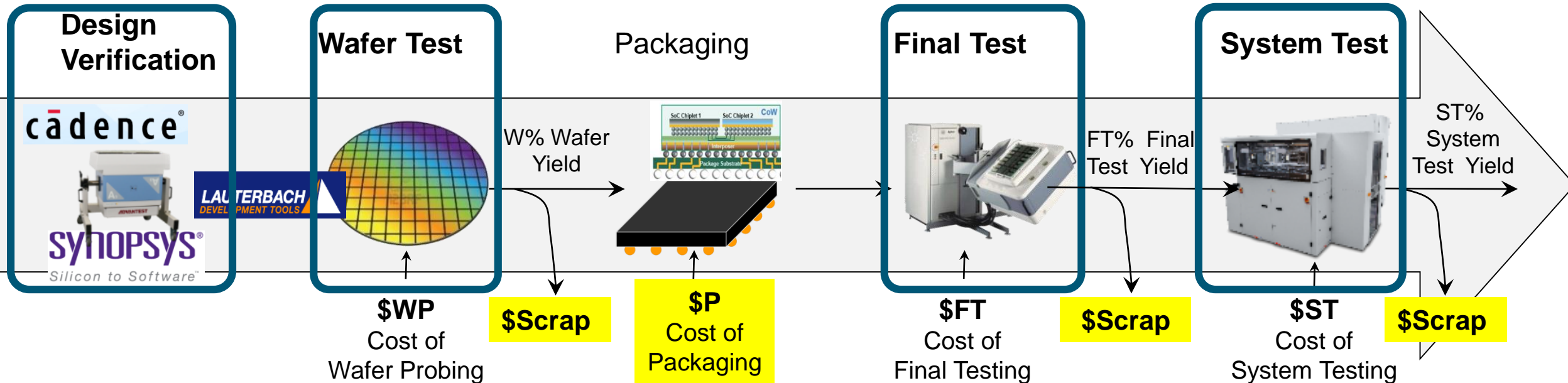
Automated EDA flow
Data Collection
System Test Cases

On-Die System Test
SoIC/CoWoS/Chiplets
Scan through functional IO
USB/PCIe/1149.10
Yield Learning

Massive Parallel Test
x16 → x24 → x32
Reduced Pin Count

Scan Over HSIO
Scan over PCIe/USB
1149.10
System Test

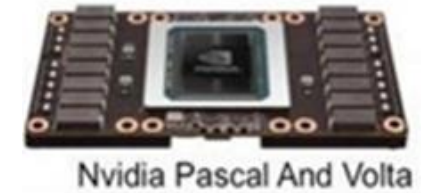
System Level
System Level test incl.
Peripherals
Only affordable if high
coverage of previous steps



Key Takeaway

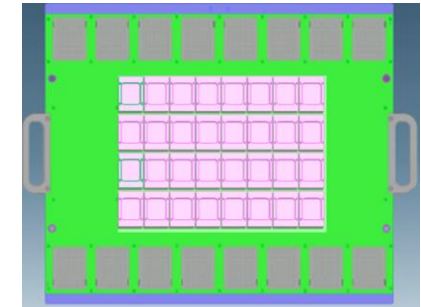
1. Need a proven, scalable and flexible test solution

- Device complexity will grow
- Heterogenous integration → incl power, precision analog, HSIO, RF



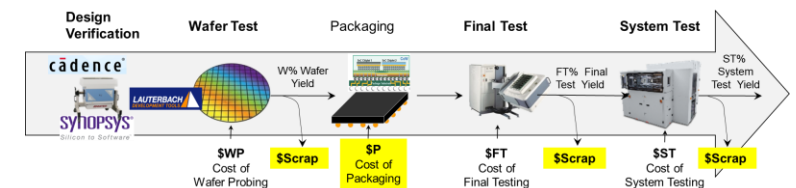
2. New test methodologies will be required

- On-die system level test
- Scan test over HSIO
- Bigger is not necessarily better



3. Optimized workflow

- Test cell with active thermal control >>500W
- Need for die level prober?
- Smarter SLT with joint ATE test strategy



4. Challenging, but promising future ...

- Building a connected & intelligent world will drive innovation and growth



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...cts[one.name].select
print("please select exact...

...on classes
...ner...
```

Questions?

contact: martin.dresler@advantest.com