Challenges In High Voltage IC Design for ATE Applications

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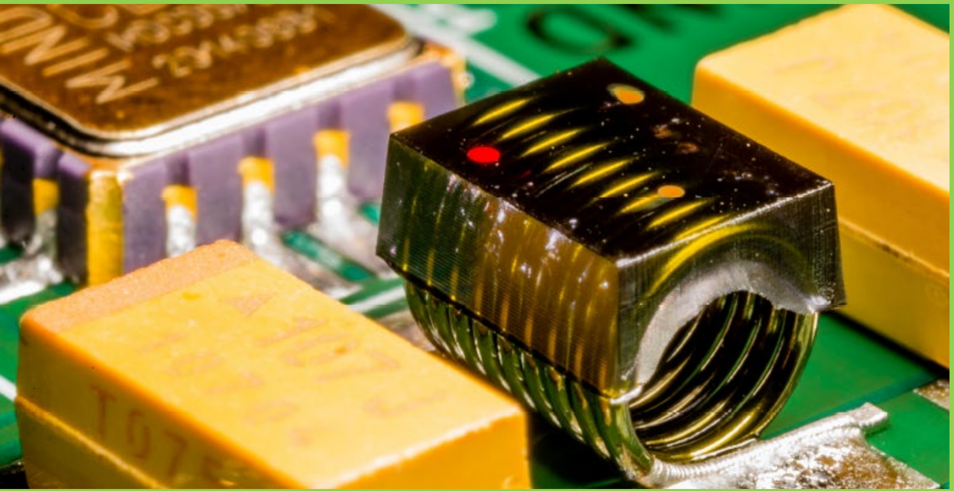
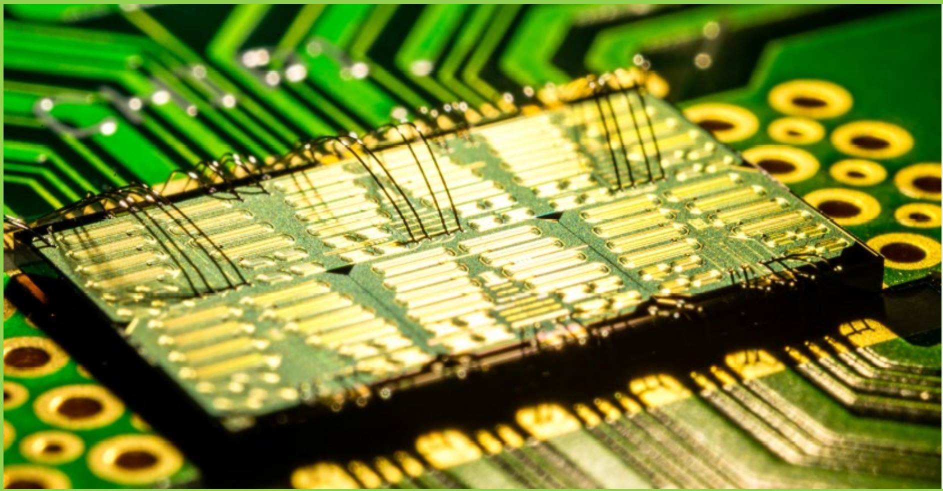
Test Technology Symposium 2019
Jef Thoné – Mike Wens

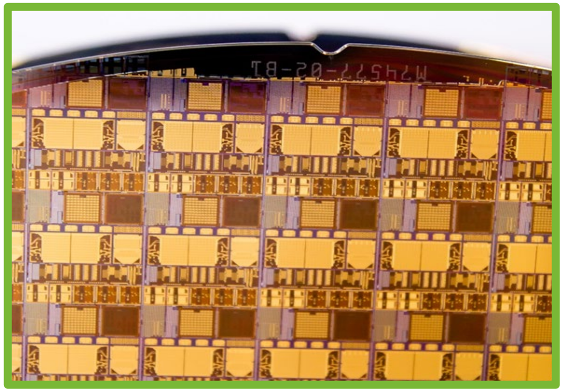
kiwa
ISO 9001 QUALITY
QUALITY MANAGEMENT



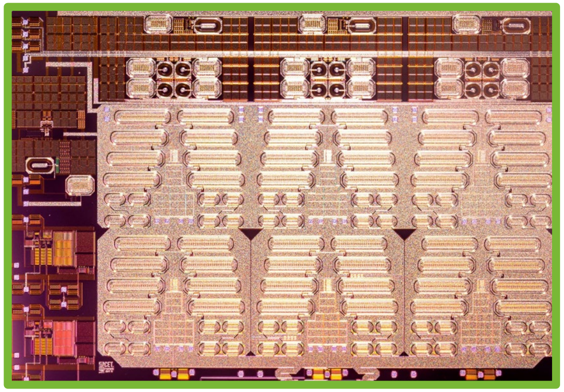


MinDCet : Power Conversion ASIC Design and Production, ISO9001

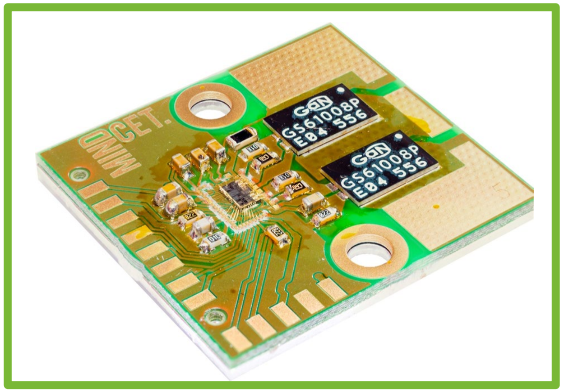
Turnkey Power ASIC Production



ASIC Design and Layout



Power Module Development



MADMIX/MADCAP

Inductor/capacitor measurement

Measurement capabilities

In house

- Recent Investments Q2 2019:
  - Teradyne ETS-88 ATE for smooth flow from characterization to production testing
  - Chroma FT3110S pick & place handler for small-volume in-house tri-temp (-40°C-150°C) testing and pre-production testing
  - Available from Q4 2019

Measurement systems under development

- **MADCAP** : non-linear large signal capacitor measurements, expected Q1 2020
- **MADTHOR** : 200V transistor analysis system (capacitance analysis and transistor curves), Q2 2020

EU Targets Greenhouse Gas Emission

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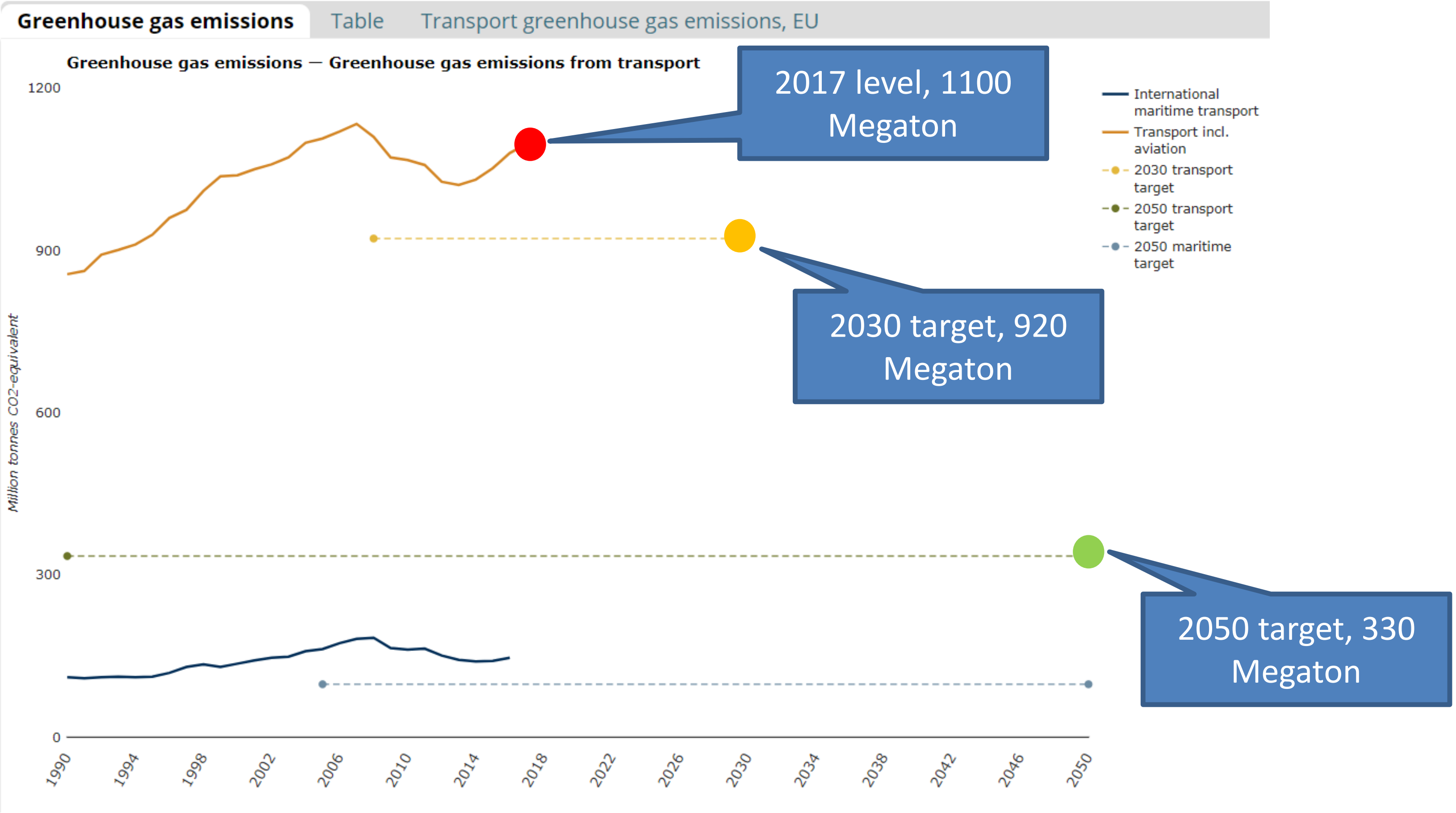
Fig. 1: Greenhouse gas emissions from transport



2017 level, 1100 Megaton

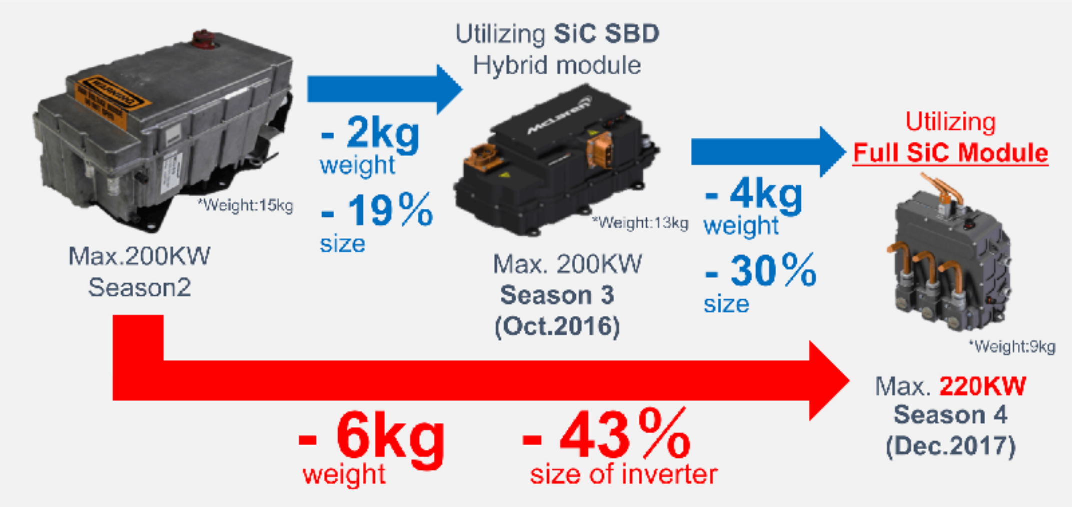
2030 target, 920 Megaton

2050 target, 330 Megaton

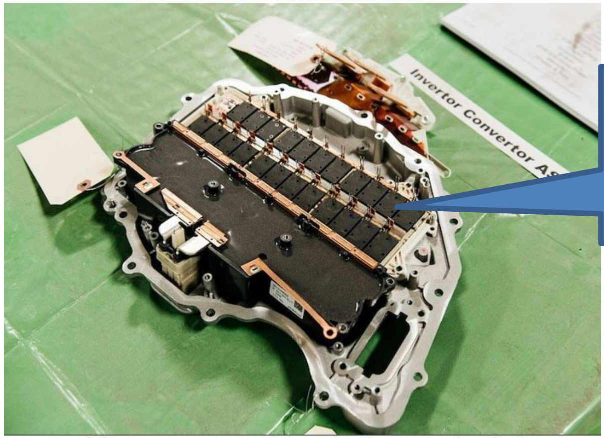
https://www.eea.europa.eu/data-and-maps/indicators/transport-emissions-of-greenhouse-gases/transport-emissions-of-greenhouse-gases-11

EV and WideBandgap

X-factor applications



Source : ROHM



Model 3 inverter. Note two rows of rectangular devices

Taken from Motor Trend photos of Munro Ass. teardown

ST / Cree SiC FETs

Source : https://cleantechnica.com/2018/05/28/more-tesla-model-3-powertrain-fun-from-carburetors-to-carborundum-youve-come-a-long-way-baby/

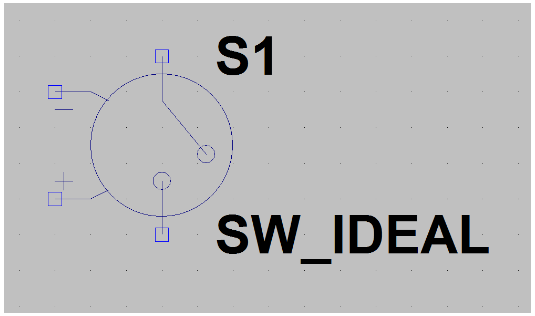
WBG properties

- Adoption of WBG (wide-bandgap) materials (SiC and GaN) improve efficiency of electrical drives
  - Faster switching / less reverse recovery => reduced switching losses
  - But : specific gate driver / isolator / isolated supplies / DC bus are needed
    - 2CV with a Ferrari engine: bad idea

- ATE need to have similar or better specs than supporting WBG components

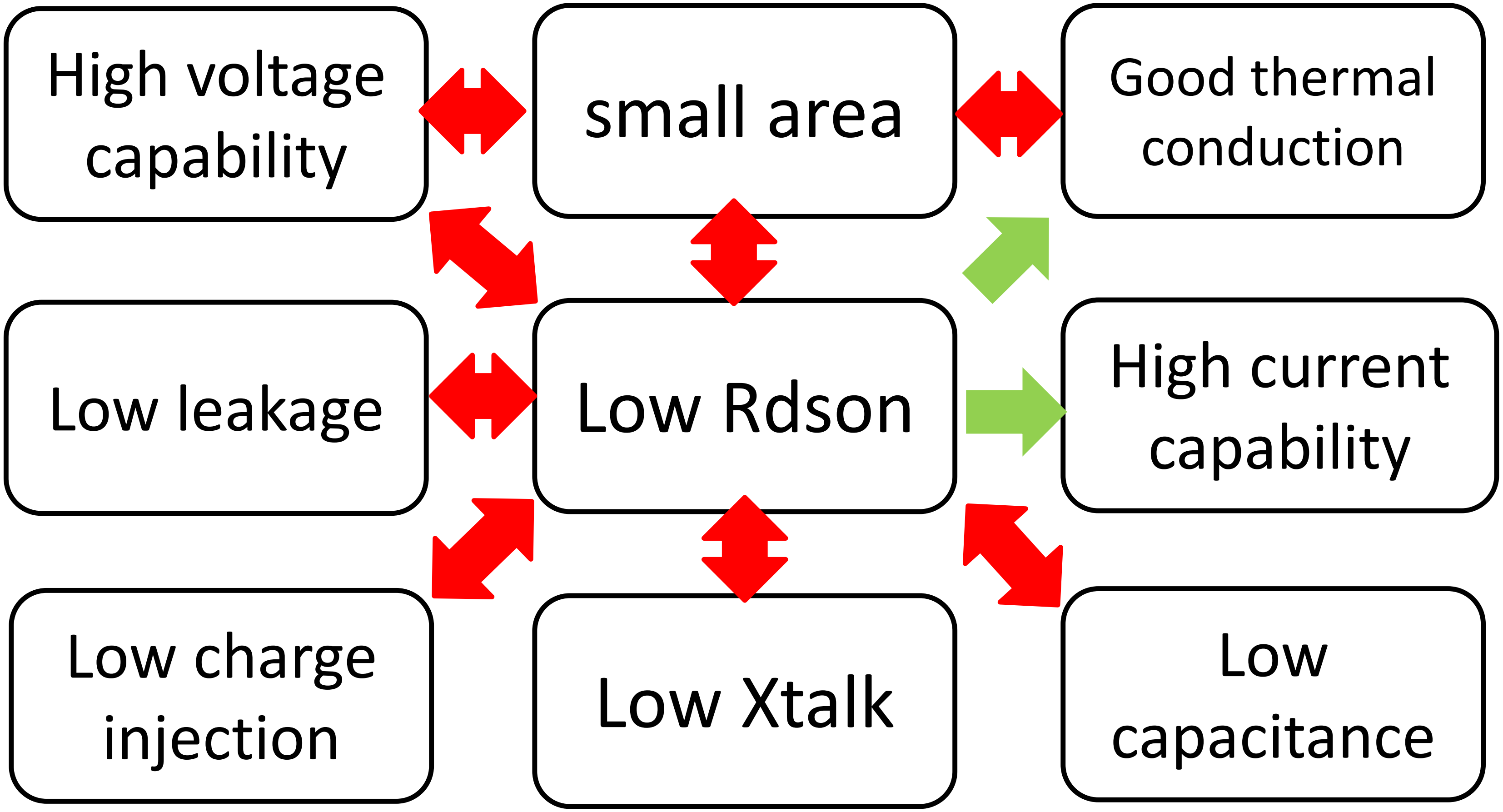
Ideal interface switch

- $R_{on} = 0$
- $R_{off} = \text{inf.}$
- $L = 0$
- $C = 0$
- Imax = Inf
- Vmax = inf.
- Area = 0
- Rth = 0



Luckily for us only in Spice…

Opposing interface requirements



What is a good compromise?

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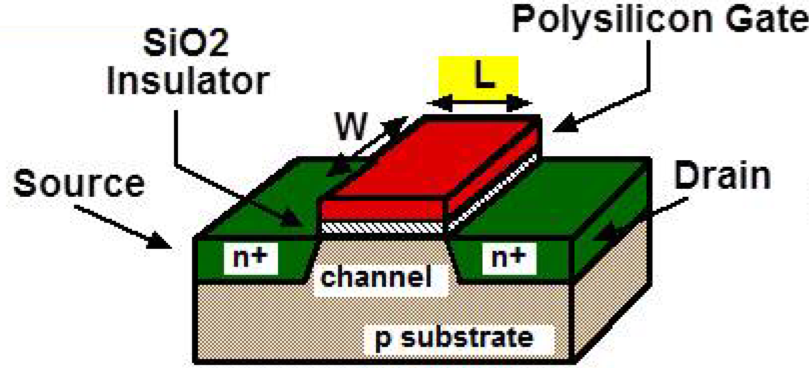
Low R_{dson}

- Rationale :
  - Conduction losses
  - RC
  - Diode conduction at rated I
- By :
  - Large W/L : R_{dson} ~ L/W
- Dependencies:
  - Area ~ L*W (cost)
  - Interconnect (metallization and bonding)



High current capability

- Rationale:
  - Conduct current within EM limits
- By:
  - Distributed current
  - Custom layout
  - Common sense + FEA
    - R3D (Silicon Frontline)
    - Magwell
- Dependencies:
  - Metallization EM limits
  - Area / aspect ratio
  - Packaging

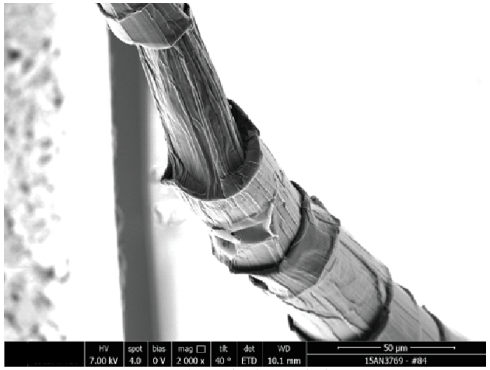
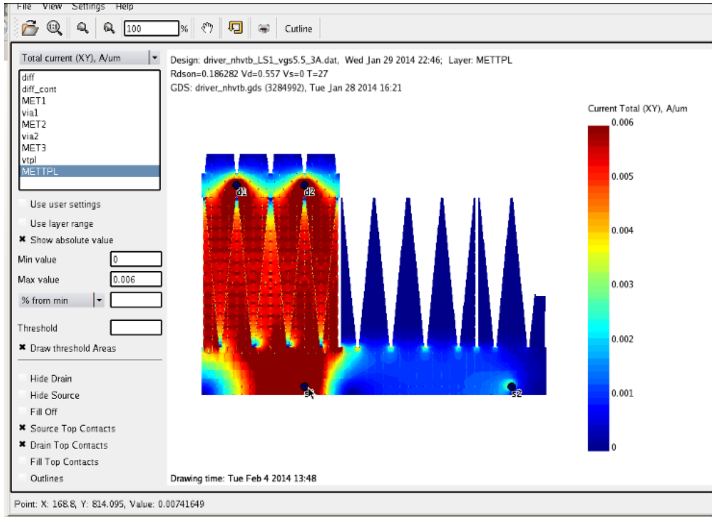


Figure 9 SEM picture of a device that has reached a resistance increase of



Total current (XY), A/um

diff
diff_cont
MET1
via1
MET2
via2
MET3
vtpl
METTPL

☐ Use user settings
☐ Use layer range
☒ Show absolute value
Min value: 0
Max value: 0.006
% from min
Threshold
☒ Draw threshold Areas
☐ Hide Drain
☐ Hide Source
☐ Fill Off
☒ Source Top Contacts
☒ Drain Top Contacts
☐ Fill Top Contacts
☐ Outlines

Design: driver_nhvtb_LS1_vgs5.5_3A.dat, Wed Jan 29 2014 22:46; Layer: METTPL
Rdson=0.186282 Vd=0.557 Vs=0 T=27
GDS: driver_nhvtb.gds (3284992), Tue Jan 28 2014 16:21

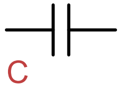
Drawing time: Tue Feb 4 2014 13:48

Point: X: 168.8, Y: 814.095, Value: 0.00741649

Small Area

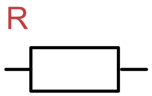
- Rationale
    - Multi channel integration
    - Low C, L and R
- By
    - Architecture
    - Technology (Si, GaN, SiC, hybrid, …)
- Dependencies
    - Die yield ~ exp^-Area
    - Thermal conduction ~ Area

1nH/mm



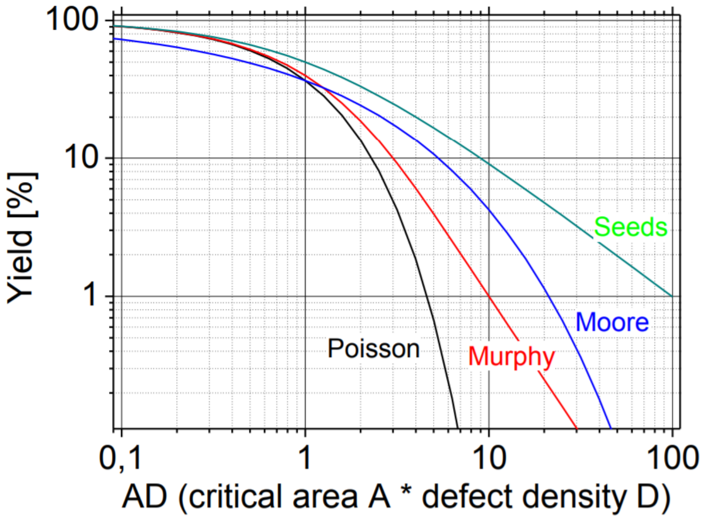
80fF/mm

1mm wide PCB trace, 1mm above ground



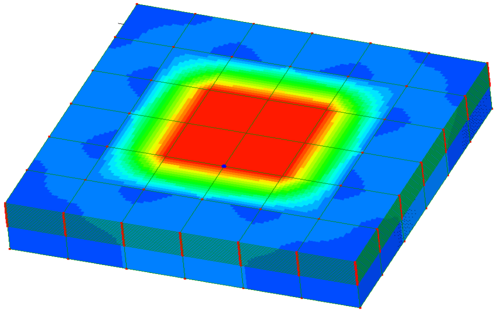
0.5mOhm/mm

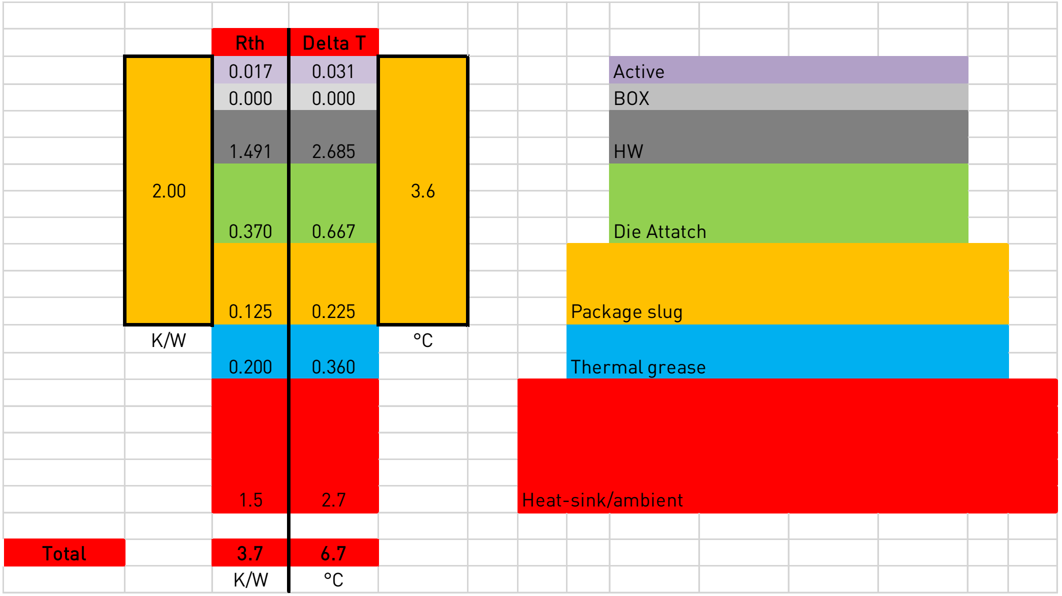
1mm wide PCB trace, 35u thick



Good thermal conduction

- Rationale:
    - Keep Tj under control (lifetime)
- By:
    - Area/dimensions
    - material stack
    - Package choice
    - FEA thermal simulation (transient/static)
- Dependencies:
    - Transient power peaks
    - Driver location
    - Thermal interface materials
    - Tech choice



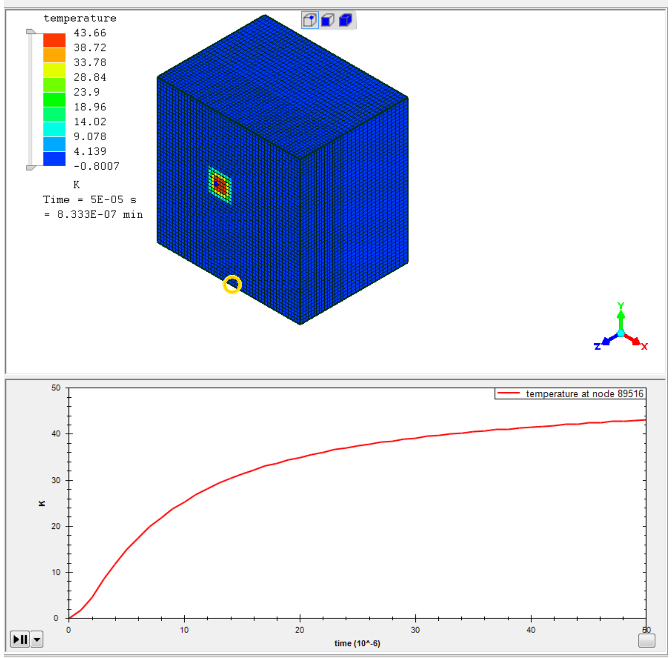


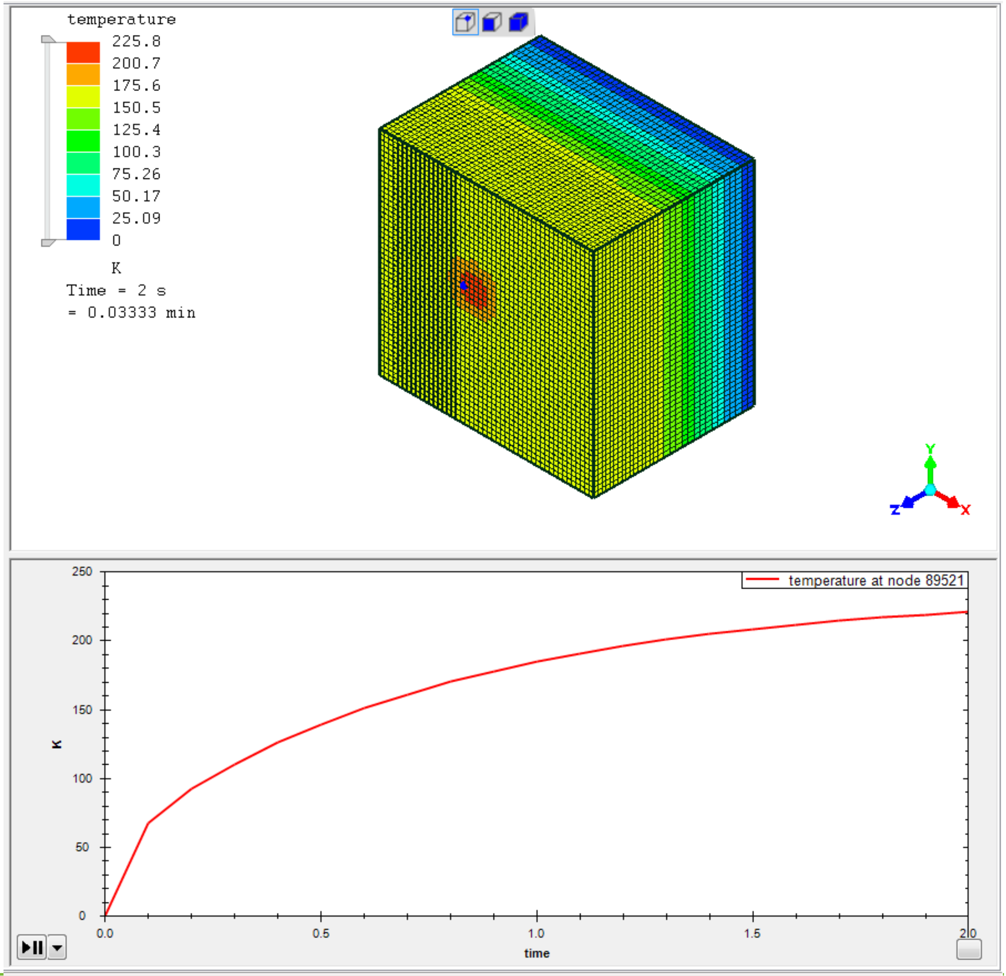
		Rth	Delta T		
	2.00	0.017	0.031	3.6	Active
		0.000	0.000		BOX
		1.491	2.685		HW
		0.370	0.667		Die Attatch
		0.125	0.225		Package slug
	K/W	0.200	0.360	°C	Thermal grease
		1.5	2.7		Heat-sink/ambient
Total		3.7	6.7		
		K/W	°C		

Good thermal conduction

E.g. 0.06mm² driver on 4mm² Si die

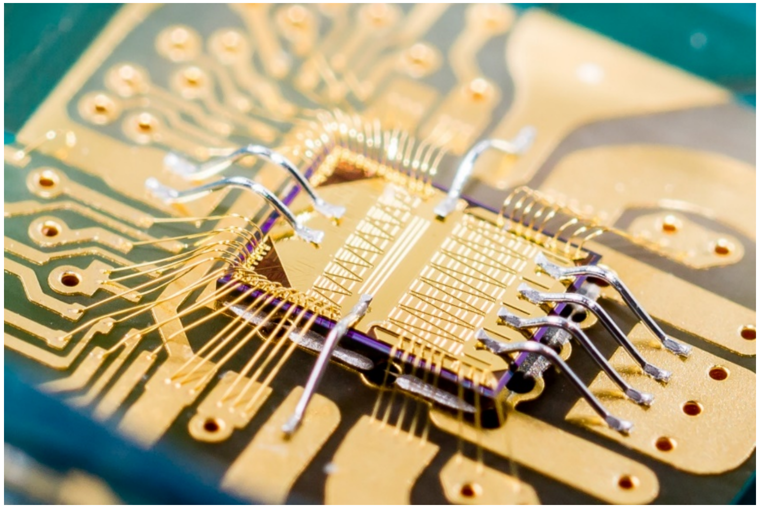
- dT @ 2us = 4.5 K
- dT @ 2 s = 225 K

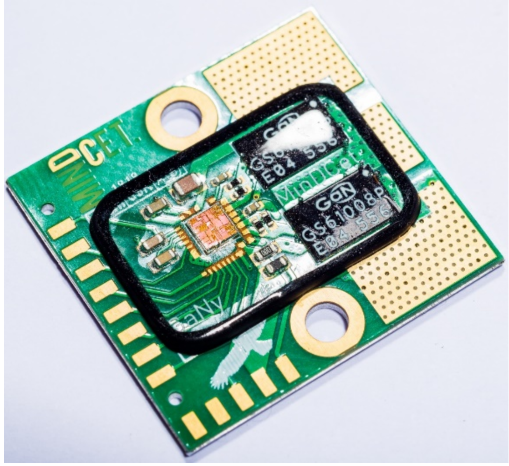


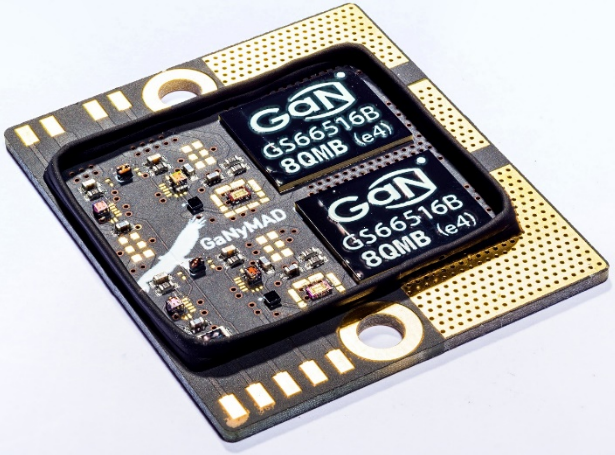


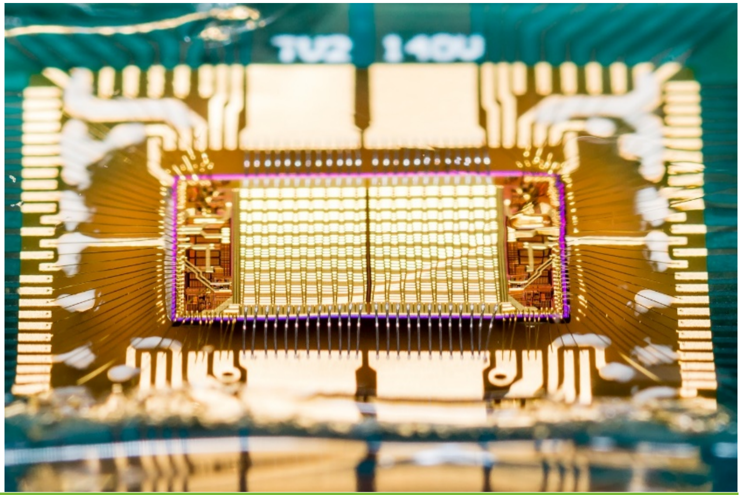
Good thermal conduction

Packaging is key



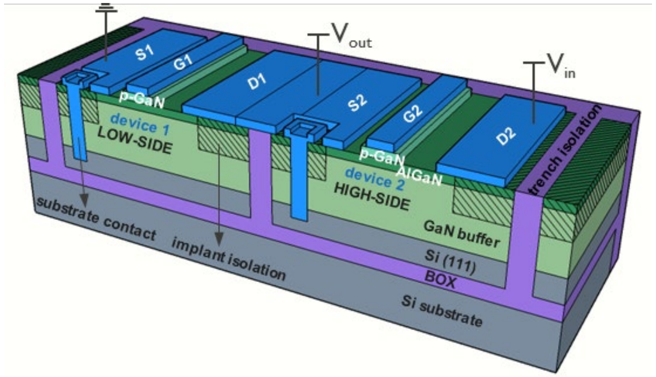




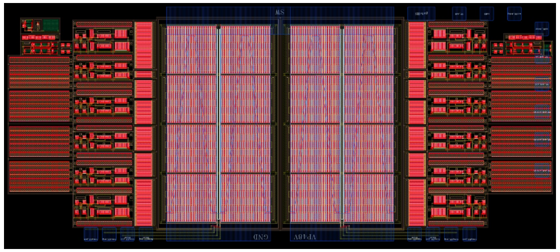


High Voltage Capability

- Rationale:
    - Meet the DUT voltage requirements
- By:
    - Technology choice
    - Custom layouts (metal clearances)
    - Custom devices
    - Custom DRC
    - Hybrid technologies (e.g. GaN-on-SOI)
- Dependencies:
    - ~ Area
    - SOA operation
    - Isolation
    - Clearance / creepage beyond package
    - ⇔ thermal requirements



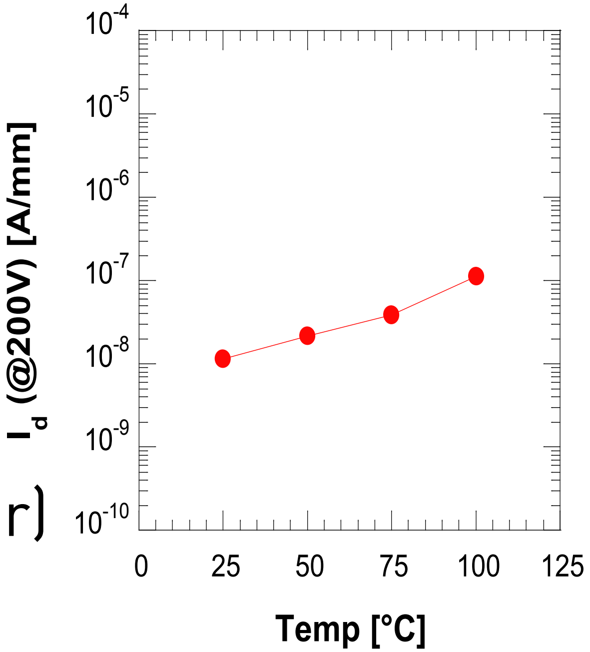
Schematic cross-section of GaN-on-SOI structure, featuring buried oxide, oxide filled deep trench, local substrate contact and p-GaN HEMT devices. Picture courtesy IMEC.



Floorplan of the symmetrical GaN-on-SOI 32 mOhm/10A halfbridge

Low leakage

- Rationale:
    - Loading of Hi-Z DUT
    - Accuracy of VI measurements
- By:
    - Technology choice
    - Architectural choices
    - Leakage cancellation circuits (1st order)
    - Calibration
- Dependencies:
    - ~ Area
    - ~ Exp(Temperature)

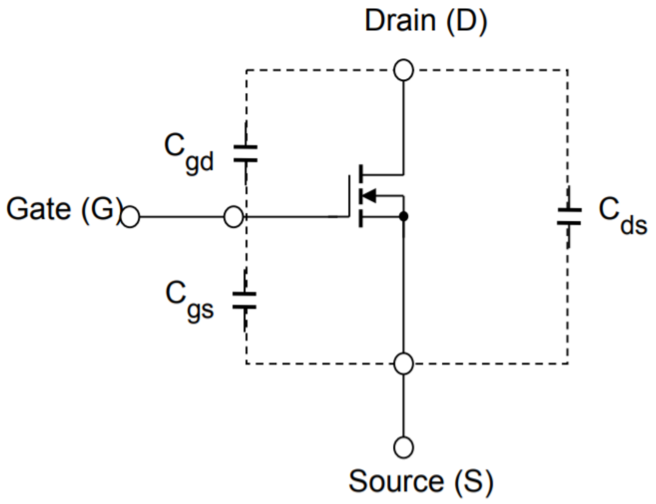


GaN on SOI 200V FET Leakage (IMEC)

Low charge injection

- Rationale:
  - Limit loading of DUT

- C_{iss} ➔ defines gate switching losses
- C_{oss} ➔ defines output switching losses
- $C_{rss} = C_{gd}$
- All non-linear vs ds/ gs voltage



Input capacitance $(C_{iss}) = C_{gd} + C_{gs}$

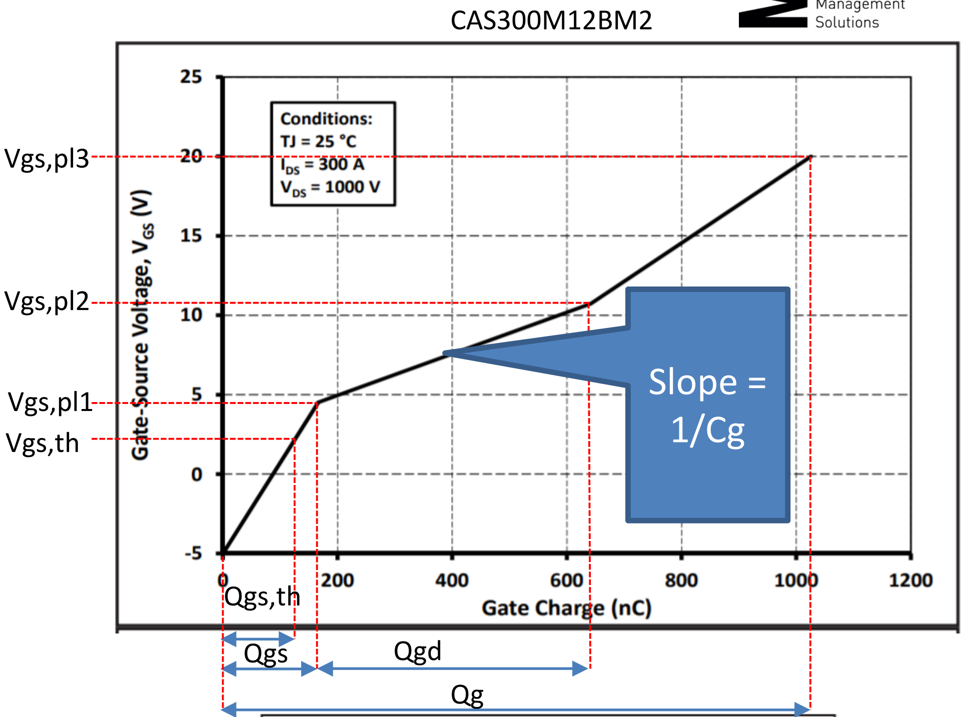
Output capacitance $(C_{oss}) = C_{ds} + C_{gd}$

Reverse transfer capacitance $(C_{rss}) = C_{gd}$

Definitions of charges

JEDEC standard 24-2

- $Q_g = Q_{gs} + Q_{gd} + C_{gs} * (V_{gs,pl2} - V_{gs,\ pl3})$
    - $Q_{gs,th} = C_{iss} * V_{gs,th}$
    - $Q_{gs} = C_{iss} * V_{gs,pl1}$
    - $Q_{gd} = C_{gs} * (V_{gs,pl1} - V_{gs,pl2}) + \int C_{dg}(V).dV_{ds}$
- $Q_{ds} = \int C_{ds}(V).dV_{ds}$
- $Q_{ci} = Q_{gd} + Q_{ds}$
- Dependencies:
    - Area
    - Technology defined!
    - Independent of switching speed!



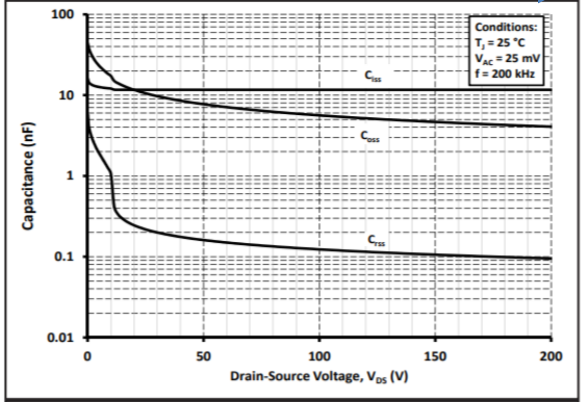
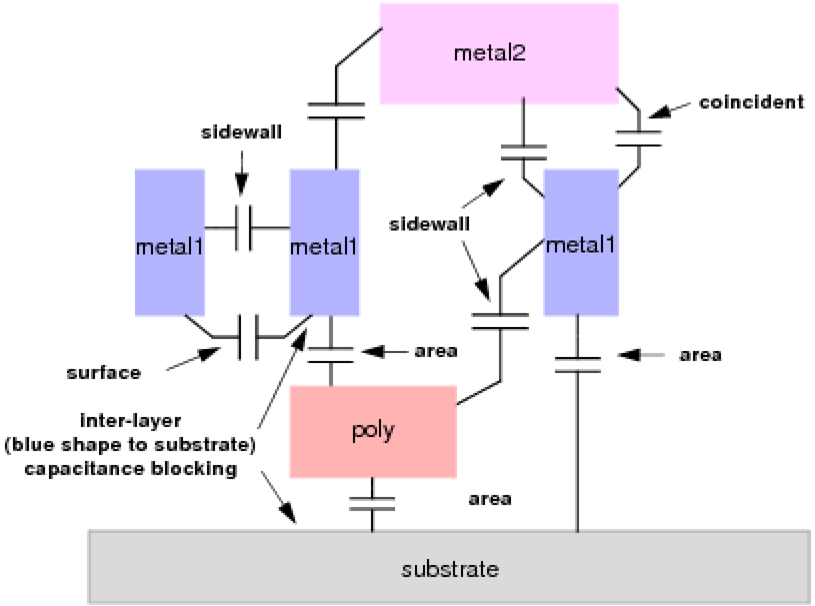


Figure 16. Typical Capacitances vs. Drain-Source Voltage (0 - 200 V)

Low capacitance

- Rationale:
  - Limit capacitive loading on the DUT
  - Limit charge injection
    - Routing can contribute up to 300%
- By:
  - Parasitic extraction, post layout
  - Smart layout strategies
- Dependencies:
  - Process metal stack



Low crosstalk

- Rationale:
  - Limit distortion of adjacent DUT channels
  - Limit loading of high impedance DUT channels
- By:
  - Limit interface capacitance
  - Low impedant return paths
  - Post layout extraction
- Dependencies:
  - Metal stack
  - Routing impedance

Conclusions

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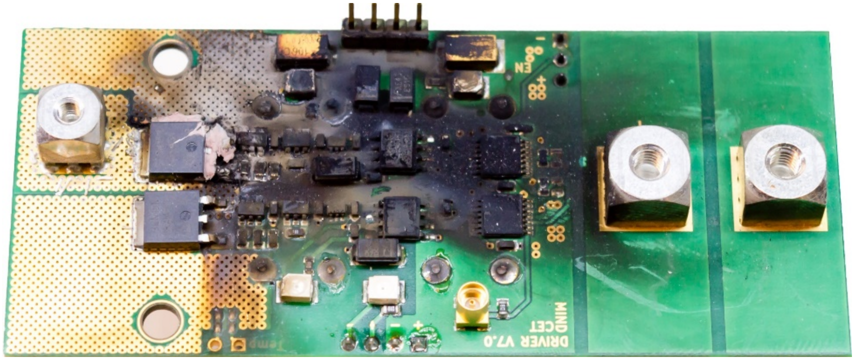
- New technology adoption (SiC/GaN) defines future ATE interface requirements
- IC Design of VI's and MUXes for ATE: multi-dimensional design challenge
- If you don't like to make trade-offs :



- If you need help to make the trade-offs: call MinDCet !

What can we do for you?

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