
# Expediting custom ASIC design & supply via proven partnerships.

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www.adestotech.com

# Agenda / Abstract

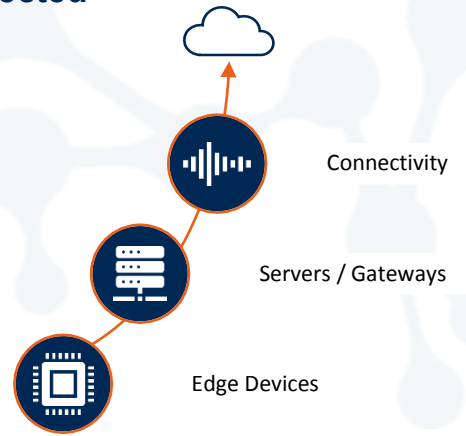
- Introduction to Adesto & our history
- Importance of partnerships & advantage of this engagement model
- Case study examples
- Conclusions

# Company Overview

## *Leading Provider of Application-Specific Semiconductors and Embedded Systems for the IoT*

**Our customers embed our innovative technologies into their solutions to enable seamless access to data and control of "things" in the connected world.**

- Founded: 2006, Silicon Valley, CA. NASDAQ: IOTS
- Long-term Supplier to Tier-1 OEMs
- Focused on High-growth IoT
- Over 5,000 Diversified Customers




**Full stack of open solutions to move data from edge to cloud**

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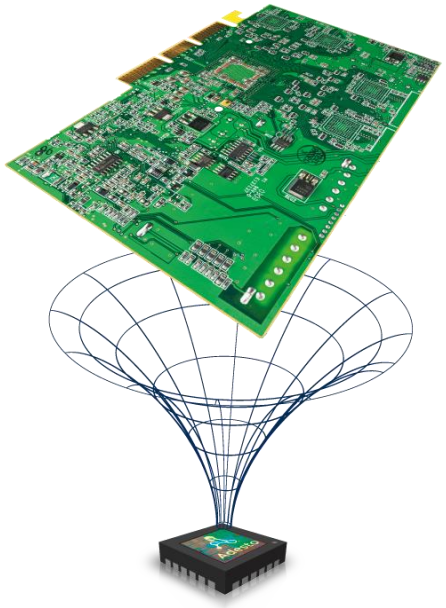
# Adesto's ASIC Mission

***We solve complex system challenges where others failed, resulting in custom chips that exceed customers' requirements***

- Performance
- Power
- System level cost



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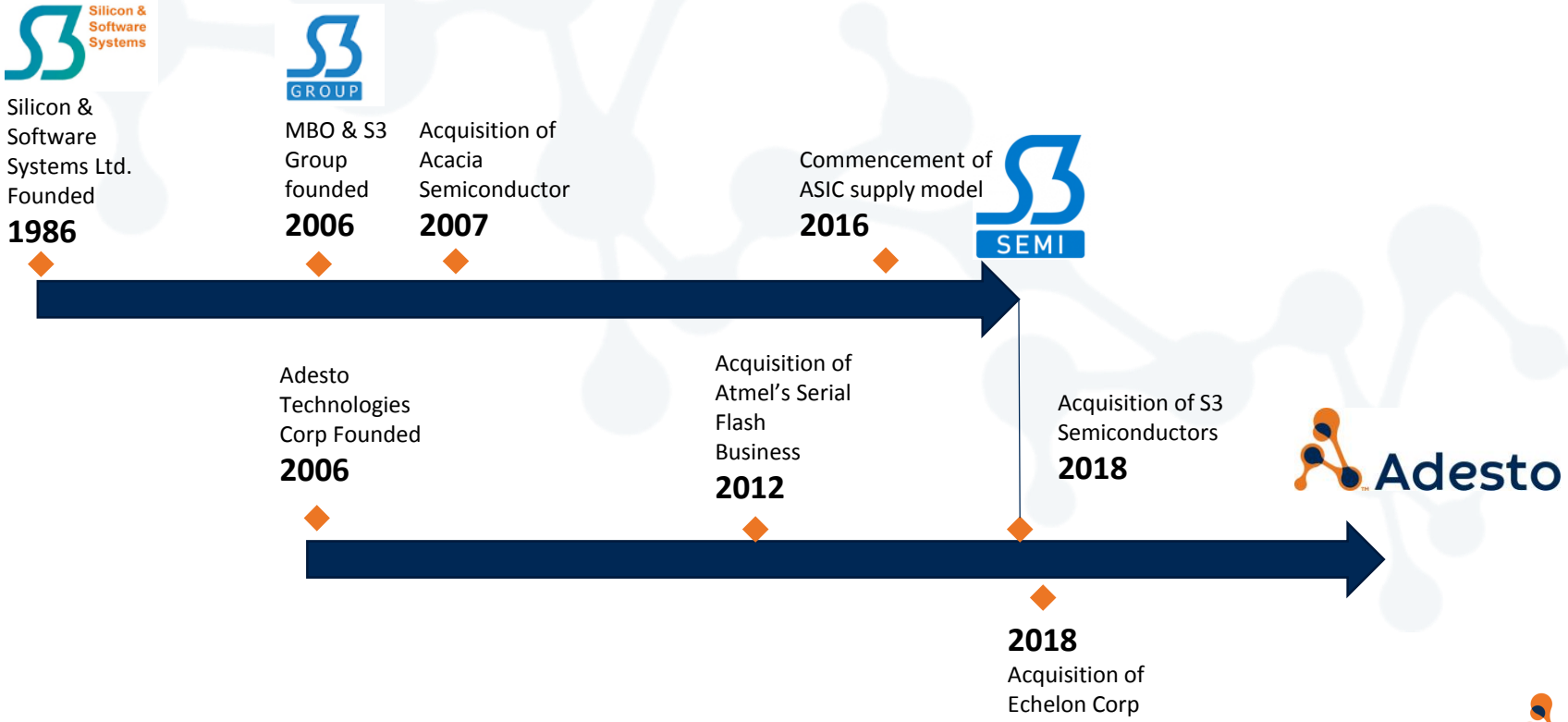
# Adesto history



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# Adesto's Worldwide Presence





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# https://www.adestotech.com/silicon-ip/

## World-class IP

For over twenty years Adesto's mixed-signal and RF design team has been developing world-class IP for use in our custom ASICs and for licensing to customers that develop their own designs.

Category: Select Value | Function: Select Value | Parameter: Select Value | Parameter: Select Value | Process Node: 40nm | Foundry: TSMC | Status: Silicon Proven

Reset All Column Filters | Copy Link

| Category | Function | IP Part # | Description | Bits / Current / Freq Low | Speed / Voltage / Freq High | Process Node | Foundry | Status |
|---|---|---|---|---|---|---|---|---|
| Temperature Sensors | Data Converters | S3ADSTS01M12BT180 | 12-bit 285kS/s SAR ADC w/ Temp. Sensor | 12 | 0.000285 | 40nm | TSMC | Silicon Proven |
| ADC | Data Converters | S3ADS1M14BT40ULPB | 14-bit 1MS/s SAR Single ADC | 14 | 1 | 40nm | TSMC | Silicon Proven |
| ADC | Data Converters | S3ADS1M10BT40ULPD | 10-bit 1MS/s SAR Single ADC | 10 | 1 | 40nm | TSMC | Silicon Proven |
| ADC | Data Converters | S3ADS1M14BT40ULP | 14-bit 1.2MS/s SAR ADC | 14 | 1.2 | 40nm | TSMC | Silicon Proven |
| LDO | Power & | S3REG10016T40LP | Low Drop Out 100mA Regulator | 100 | 2.5 | 40nm | TSMC | Silicon |




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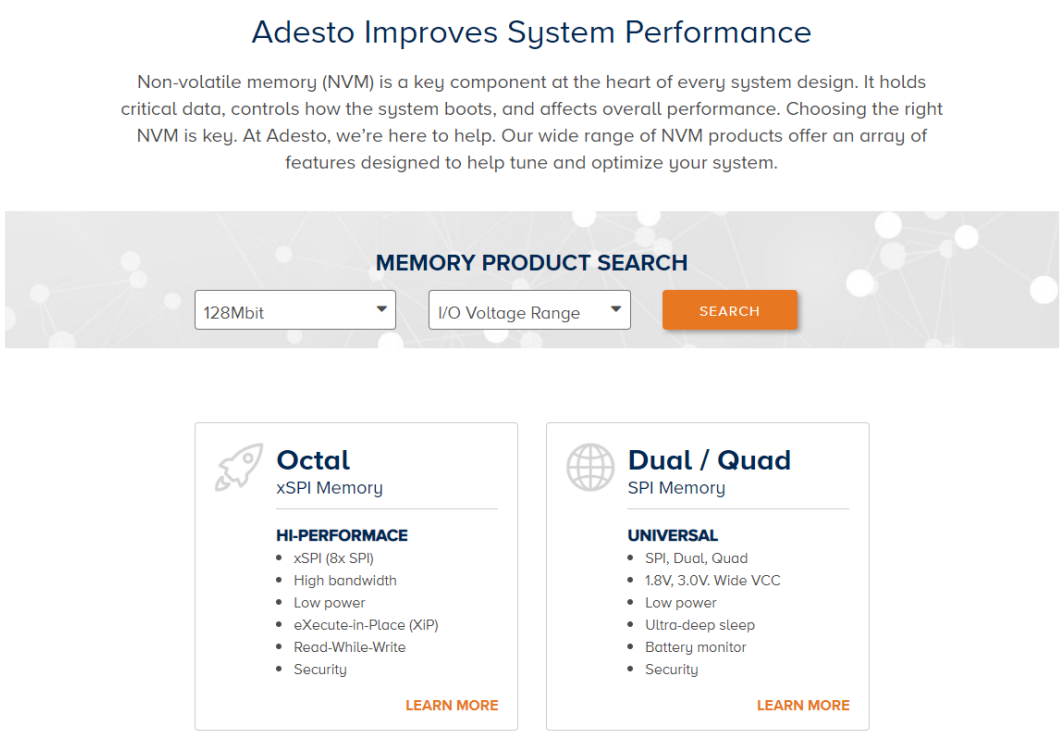
# https://www.adestotech.com/products/memory/







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# https://www.adestotech.com/products/power-line-communications/


## Features

Universal communications platform

Superior noise immunity

AES 128 / AES 256 Encryption Core

Cost Optimization peripheral Integration

Single chip PHY and MAC integration

Smart Grid, Smart Lighting and Industrial Automation applications benefit from the SM2400 series narrow band N-PLC solutions which support all worldwide OFDM modulation based standards such as G3-PLC, PRIME and IEEE 1901.2 as well as FSK modulation. The SM2480 serves as a fully integrated Analog Controller with Grid connectivity tailored to applications such as solar panel micro-inverters, smart LED controllers and other Grid-connected devices.

| Products & Datasheets | Documents | Applications | Tools |
|---|---|---|---|

| PRODUCT | DATASHEET | DENSITY | SPEED | VCC RANGE | INTERFACE | LEARN MORE / REQUEST SAMPLES | PURCHASE |
|---|---|---|---|---|---|---|---|
| SM2400 | Download | N/A | See Datasheet | Core- 1.6V-1.98V ; I/O 3.0V-3.6V | Multi | + | N/A |
| SM2480 | Download | N/A | See Datasheet | Core- 1.6V-1.98V ; I/O 3.0V-3.6V | Multi | + | N/A |




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# Adesto Centres of Expertise

- Ireland
  - Dublin – ASIC Supply, Logistics
  - Cork – RF Design, Hardware Development
- Lisbon
  - ADC Design
- Czech Republic
  - Prague - ASIC Design and Integration
  - USA
    - Santa Clara – DAC design and Memory supply


Member of TSMC Design Centre Alliance. (DCA)


ARM Approved Design Partner.




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# Why Adesto's ASIC & IP Solutions

## UNIQUE ASSETS

**300+**

*RF/Mixed-Signal IP Blocks*

**100**

*Engineers*

**15+**

*Years of Average Experience*

**10**

*Years of Average Tenure*

## RARE EXPERTISE

*Expertise in integration of analog / RF / embedded systems*

## OUR TRACK RECORD

**30+**

*Years of Delivering High-end ASICs*

**80%**

*Designs First-Time Right*




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# Adesto partnerships

- Fabless semiconductor company
- Trusted partnerships across foundry, test and packaging essential to our success
  - Customers trust Adesto to deliver on our commitment
  - Adesto trusts partners to work closely together to meet those commitments.
  - Salland key partner for our Test operations
- 3rd Party IP partnerships (ARM approved Design Partner)













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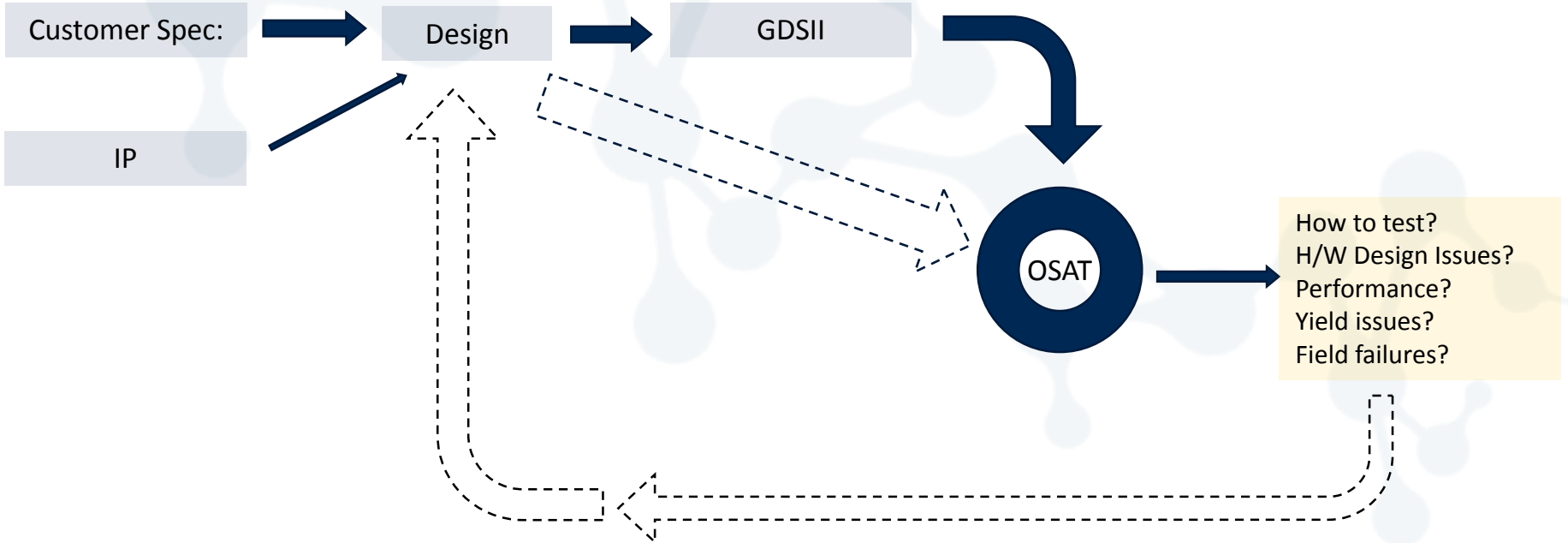
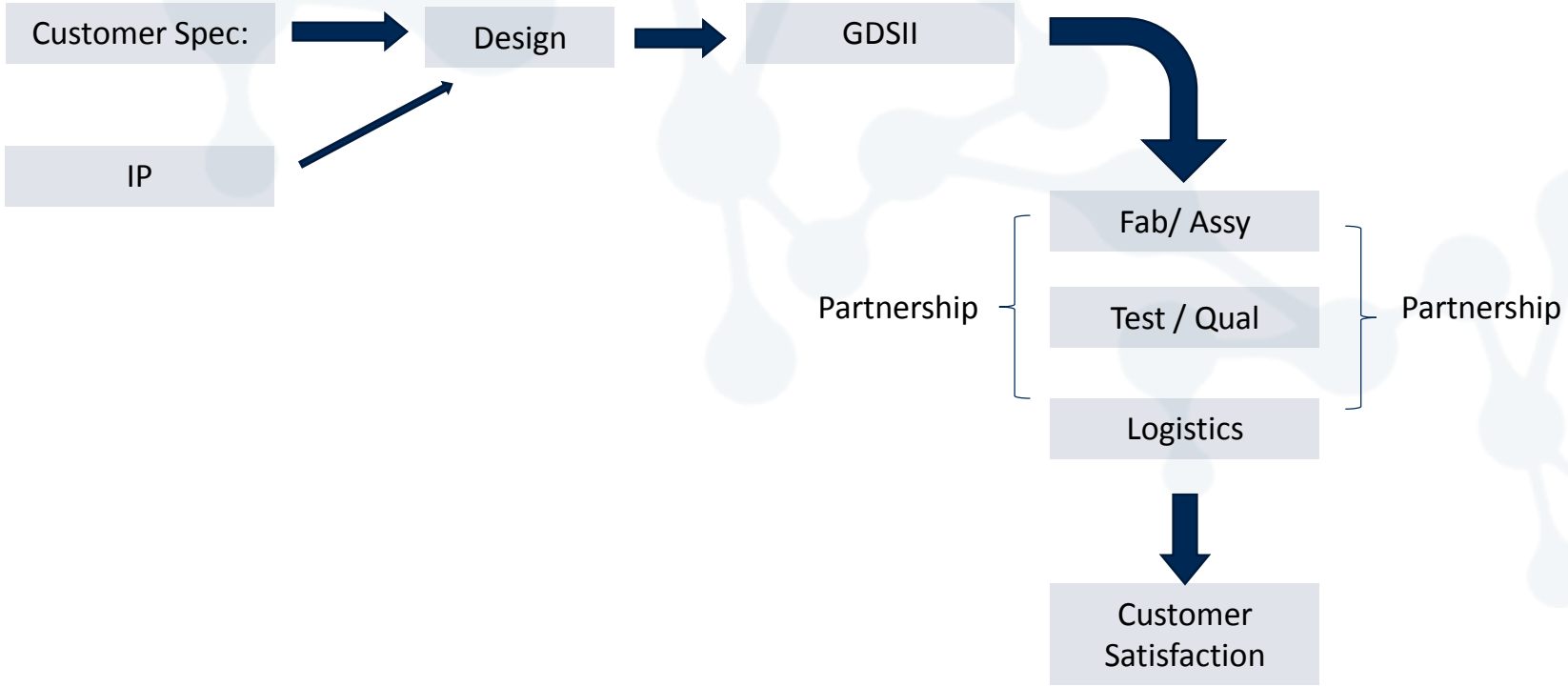
# Transition From Old to New

# Traditional Business model



# New ASIC Supply Model



# Overlapping Projects

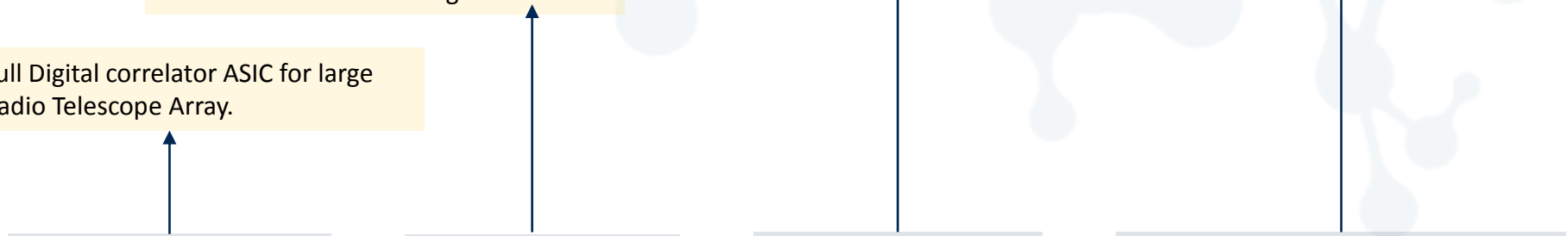
SALLAND Engineering

Interface for 5G Wireless baseband Interface between RF IC and Processor with 8x 12 bit DACs, 8 12 Bit ADCs, 2x JESD high speed serial and SERDES logic.

Satellite communications RF transceiver.
Full Duplex, dual receiver with Stacked Dual VCO

Human interface mixed signal ASIC

Full Digital correlator ASIC for large Radio Telescope Array.



Feasibility Study Phase | Quotation Phase | Development Phase | Volume Ramp Phase

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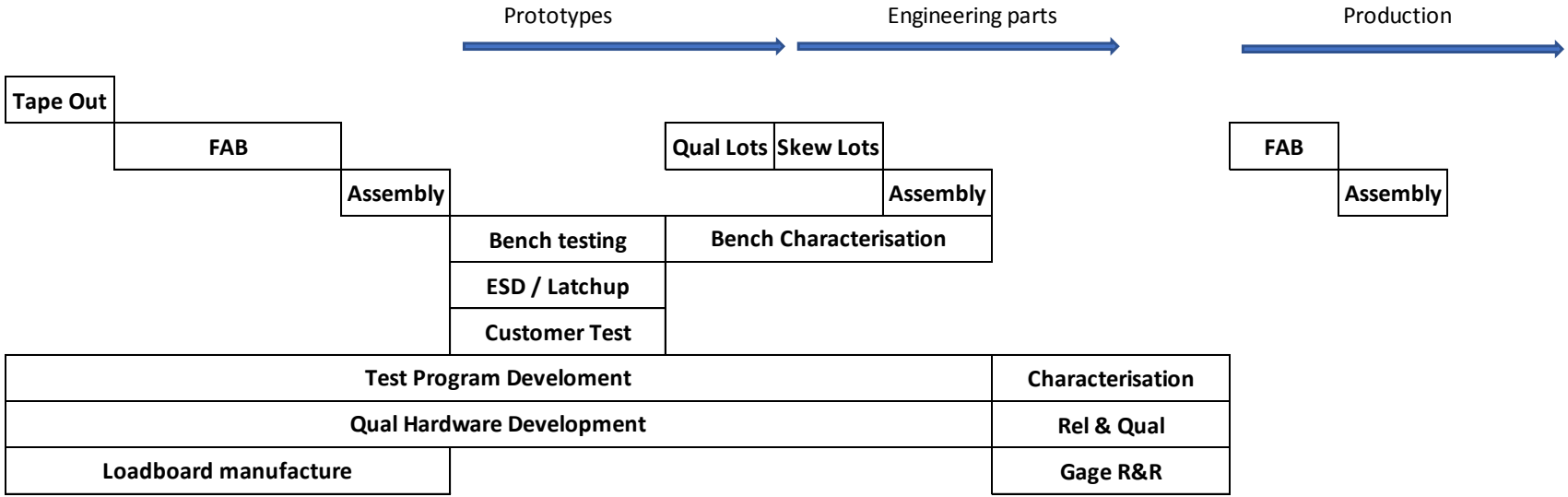
# Typical ASIC Rollout Schedule



# Case Study 1

Mixed Signal ASIC

# Mixed Signal ASIC

- This ASIC is a Mixed Signal Baseband IC Tx/ Rx with high speed serdes, that acts as an interface between an RFIC and a baseband processor.
- It was designed on a 40nm CMOS low power node at TSMC and incorporates 8 ADESTO DACs and ADCs, as well as some 3rd party IP.
- Assembled by ASE, it is a wire bond solution in a 13x13x1.4mm 221L LFBGA.
- Test development was done at Salland, and reliability was done at Maser.



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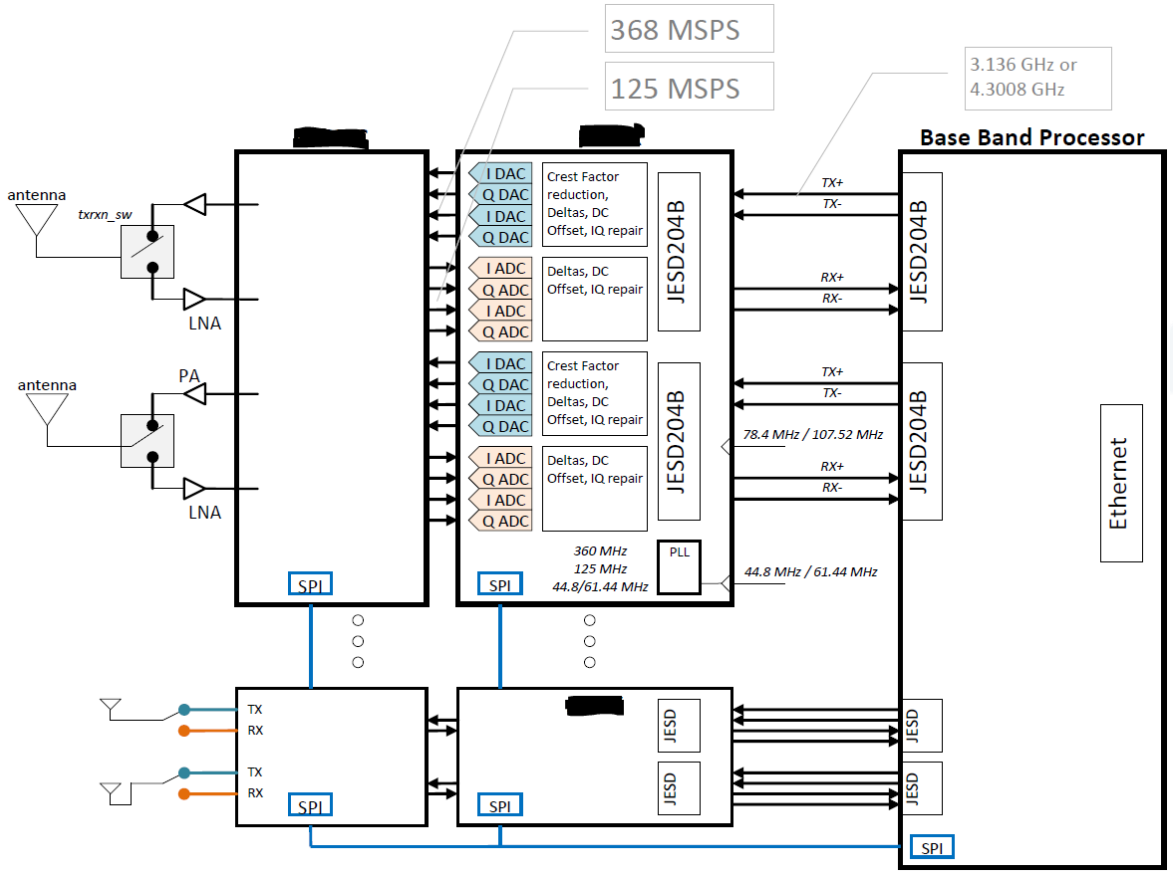
# 5G Wireless baseband Interface



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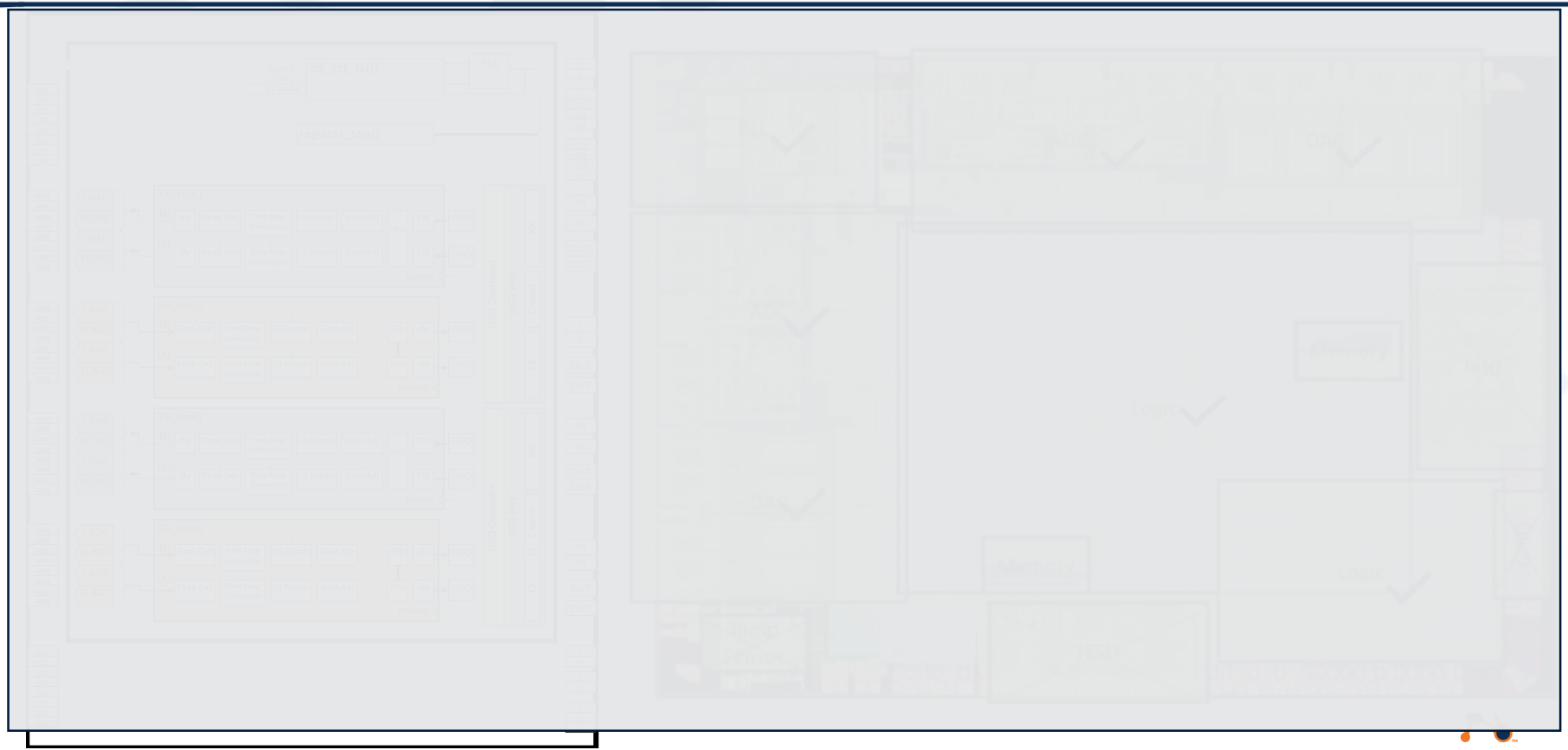
# ASIC Details



# Test Solution

- Test solution was on the Teradyne Ultraflex platform, giving us optimum parallelism and throughput.
- 4 test sites.
- DFT:
  - On board BER and PRBS
  - On board digital ramp and sine wave generators
  - Digital loopback between DACs and ADCs
  - Internal and external SERDES loopback.
  - MBIST / SCAN
- Low test time and minimum component count on Loadboard.

# Reliability and Qual

- Partnered with Maser
  - Full suite of qualification and package reliability
    - HTOL
    - Biased HAST
    - HTSL
    - TMCL
    - ESD / Latchup
- Significant challenges overcome
  - High pin count
  - High Power dissipation

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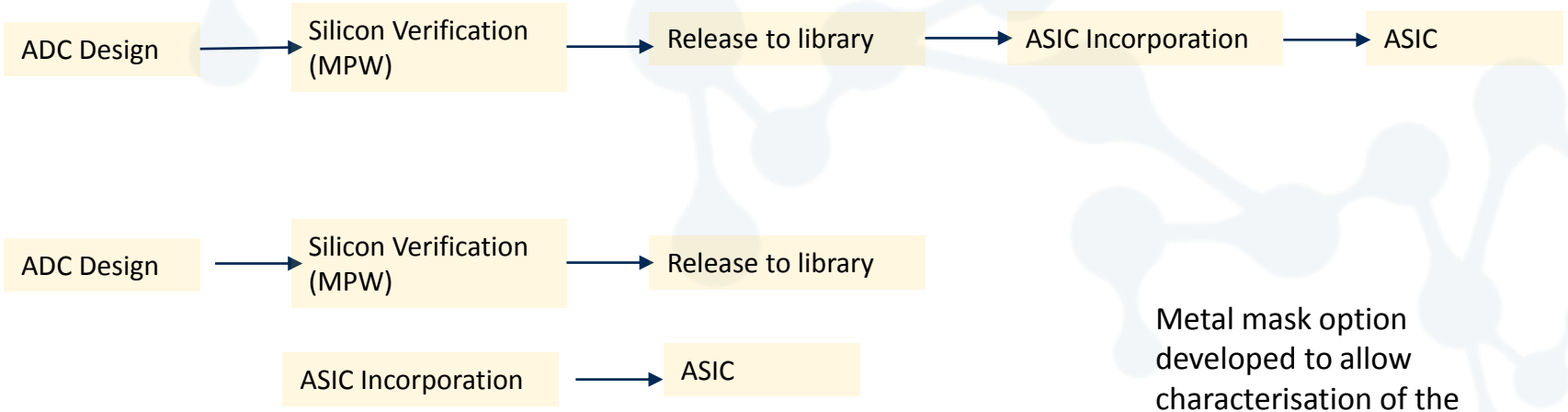
# Efficiency

- Consolidation of Test Chip & ASIC Rollout




Metal mask option developed to allow characterisation of the ADC.
This shortens the design cycle of the next ADC and /or ASIC.

# Case Study 2

RF ASIC

# RF ASIC

- This ASIC is in development.
  - Two stacked dies.
  - Customer requested a BOM reduction by adding VCO's on chip.
  - RF die originally designed by Adesto but supplied on the old OSAT model.
  - Package - 120 Pin AQFN Package (9*9mm).
- Fab: TSMC
- Assembly: ASE
- Test: Salland
- Qual: Maser



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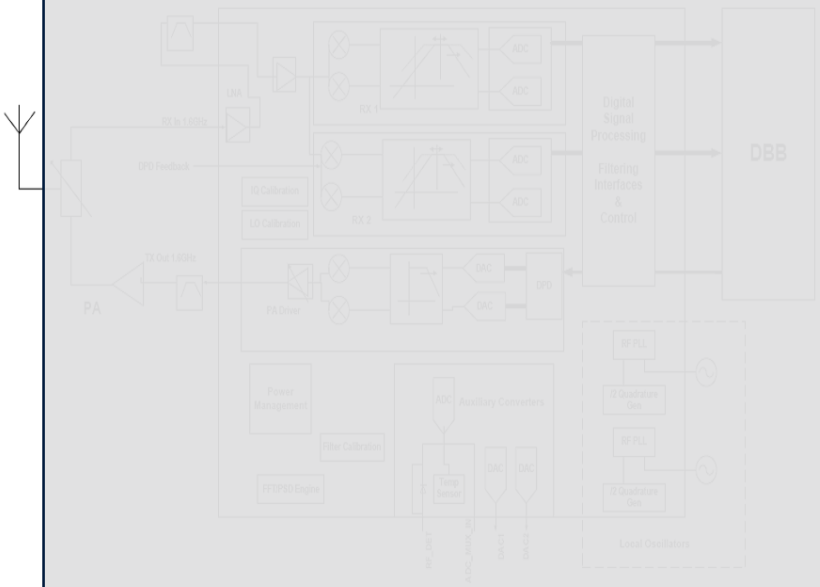
# Efficiency




Legacy Adesto / S3 Design
Using OSI model




New Adesto / S3 Design
Using ASIC Supply model

# Stacked Die Arrangement

# Test Solution

- Test solution is targeted for the Teradyne Ultraflex platform
  - Quad site, high throughput solution.
- Partnering with Salland and Maser

# Why this model works

- Proven Track record of Salland and Maser's collaboration
- Re-use of working practices
  - The overlapping nature of the projects ensures continuity of progress.
- Reuse of IP
  - Test program leverage
  - H/W designs
- Communications.
  - File transfer and release management
  - Confidentiality
- Collaboration
  - Round table Engineering with Salland, Adesto, customer engineers.



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# Conclusions

- Adesto has been developing semiconductor solutions for our customer base for over 30 years
- As a fabless company, we rely on strong relationships with our partner network
- Shortening of design cycle by use of this key partner method
  - Many advantages as shown in the case studies to having such a manufacturing model
  - Cost & time effective



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# Conclusions

- Adesto and S3 make a great combination for designing and delivering ASICs.
- The Partnership model works best for our product offerings, target markets and volumes.
- The Salland / Maser collaboration fits well into our business model.
- We have access into the foundries based on our legacy and continued generation of IP.
- Foundries are happy to work with us as we fill production capacity on their legacy process nodes.



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# Thank you

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