SALLAND Engineering
Test Technology Center

SE-DPIN: Challenges in IO channel development

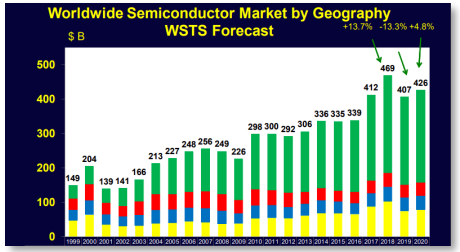
Harry Ramaker / Paul van Ulsen

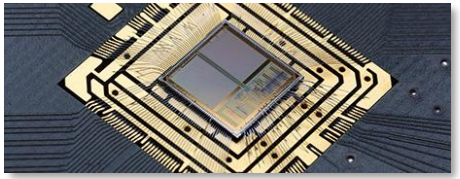
SALLAND Engineering
Test Technology Center

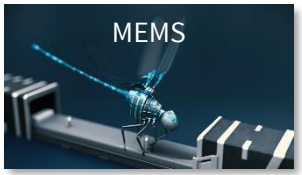
Today's Challenges

Many trends that push up development costs of ATE

- Semi market is growing but with 'ripples'
- Chip complexity increases
- ATE market is 'Stabilizing'
- Shorter life times
- New markets coming up
  - Specifications not well defined yet







Test Solution Development costs go up ➔ STTC idea born!

Typical instrument challenges

Technical

- Nothing is standard in ATE except 48V
- How to get as many channels as possible on a board within …
  - Instrument board space
  - Power, Cooling, etc.
- Easy integration with Customer platform
- Easy & Fast calibration
- Robust & Reliable

By the way… it should cost nothing, and yesterday ready ;-)

HD Instrument development requires use of ‘ATE-asics’

Another variable in the game

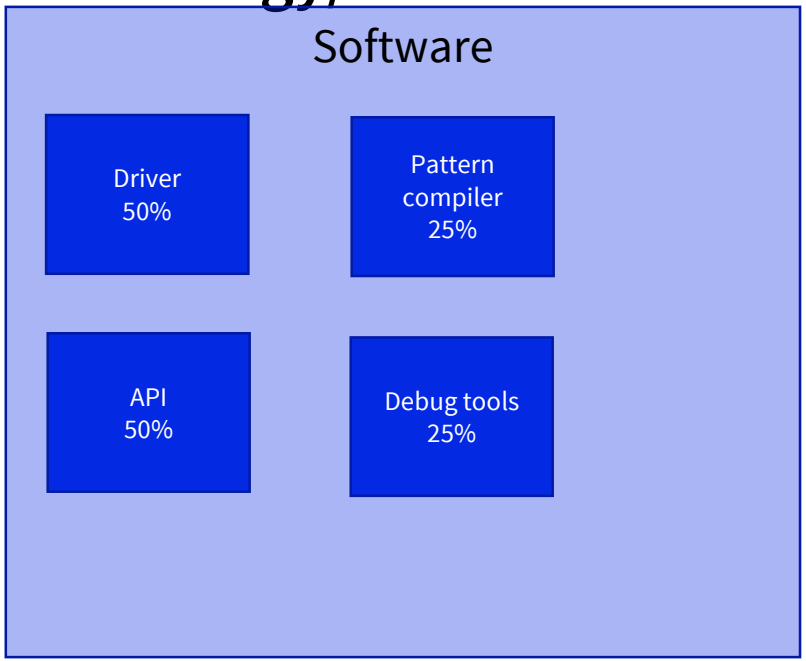
Typical development steps

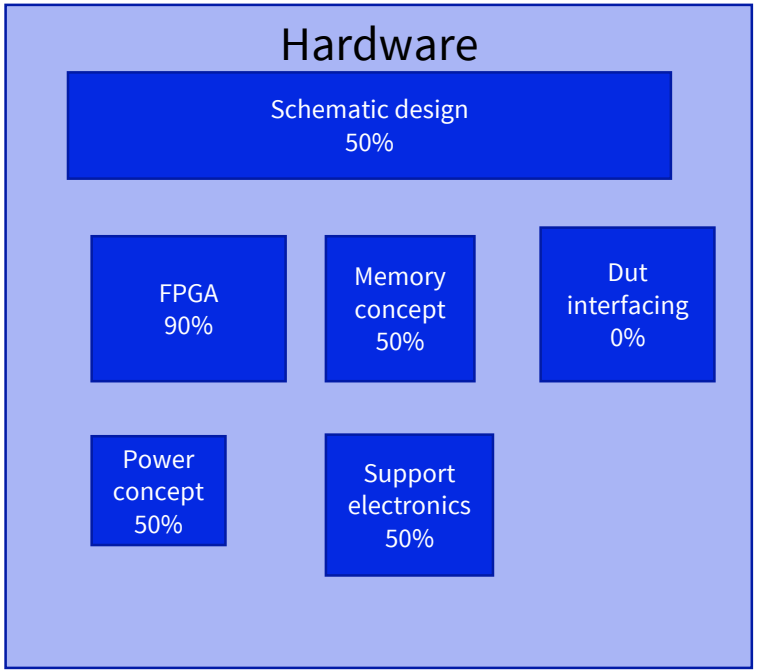
- Characterization ➔ EVM ➔ one channel PoC ➔ Instrument

Our approach

- Create high-level design
- Engage with suppliers to find new ASIC technology/developments
- Develop characterization boards
- Develop customer EVM boards
- One channel proof of concept based on EVM
- Develop complete channel

Example: Functional reuse of Salland DPIN technology/IP





High density Low cost IO - IP Project

Digital channel Building block design

Target Specification (200+MHz)

Pin Electronics Driver/Comparator (500MHz)

- Dual Mode3-level Driver with Hi-Z Capability (DVH, DVL,
- 5 Current Ranges (±2µA, ±20µA, ±200µA, ±2mA, ±50mA)
- Programmable Voltage and Current Clamps

Resistive Load Function (5 Selectable Resistor Values)

Per Pin Active Load

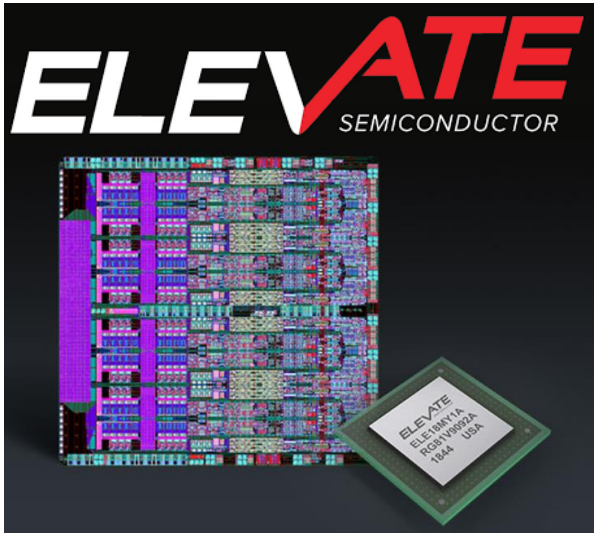
- ±24mA Maximum Current
- Independently Programmable Current Source, Current Sink and Commutating Voltage levels

Per Pin Timing Deskew

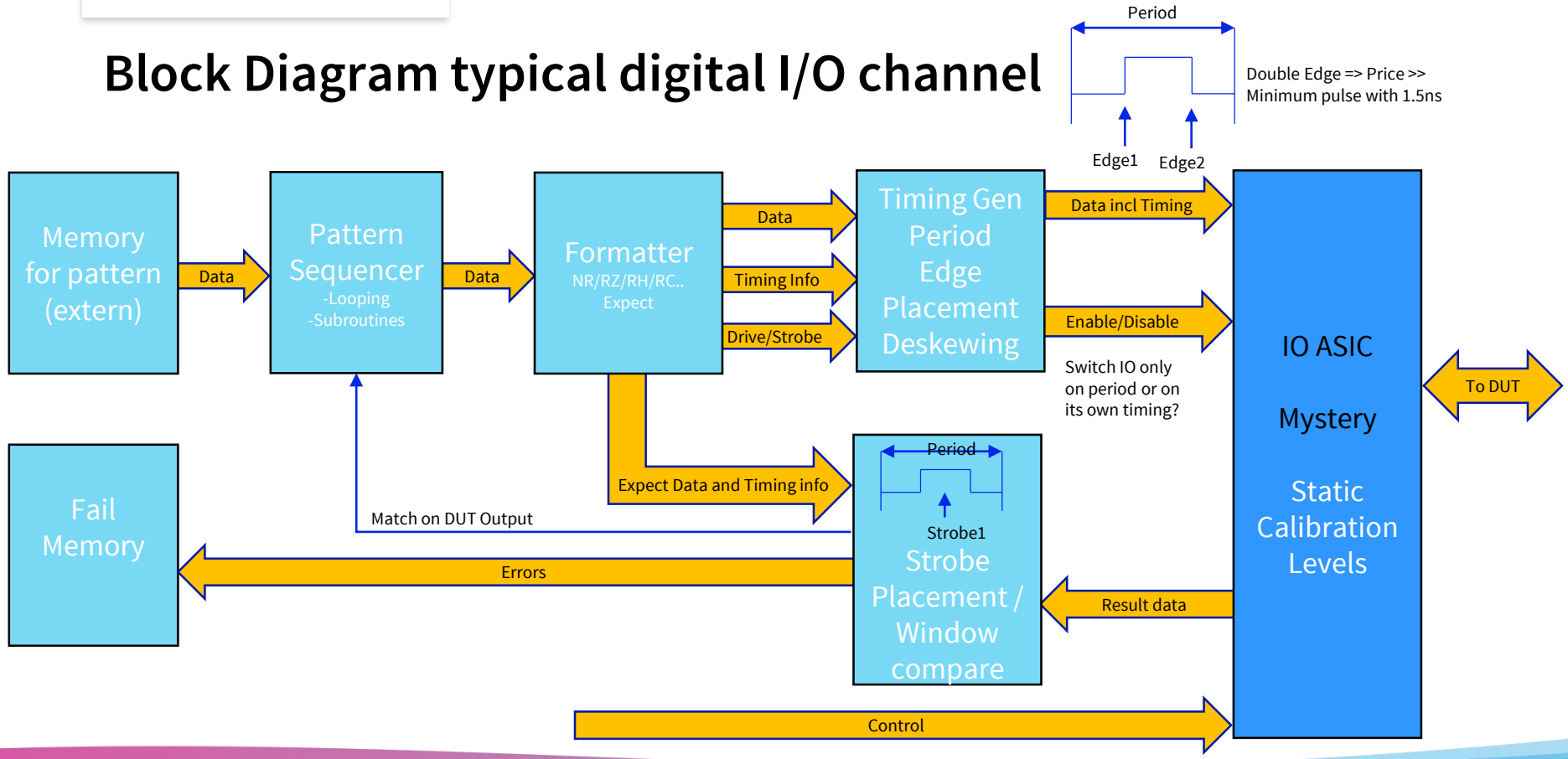
- Propagation Delay Adjustment
- 5ns Delay Adjustment Range

Per Pin PMU

- FV, FI, MV, MI
- 4 Quadrant Operation
- 2V to +6V FV/MV Range



Block Diagram typical digital I/O channel



SALLAND Engineering
Test Technology Center

SE Experience

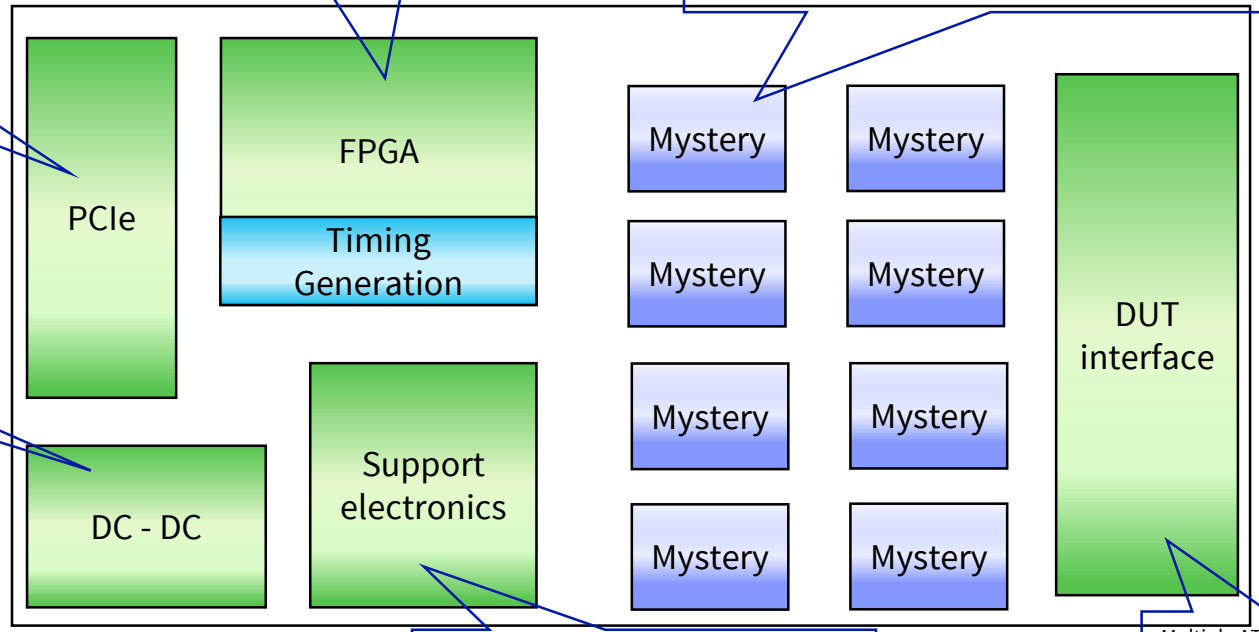
Experience with ATE instrument FPGAs
control for VI, PMU, DPS
Parallel processing
Protocol aware

Xilinx

Experience with digital I/O ATE ASICS
API, control sw, register mapping, characterization, bench board development, ATE production test solution.
We developed a Bench board for a Digital I/O ASIC for Elevate and running production of this ASIC (ATE test program)

Working on:
Mystery, Bench board design, API, Control sw
ATE test application.

Implementation of PCIe in
PC cards & ATE instruments



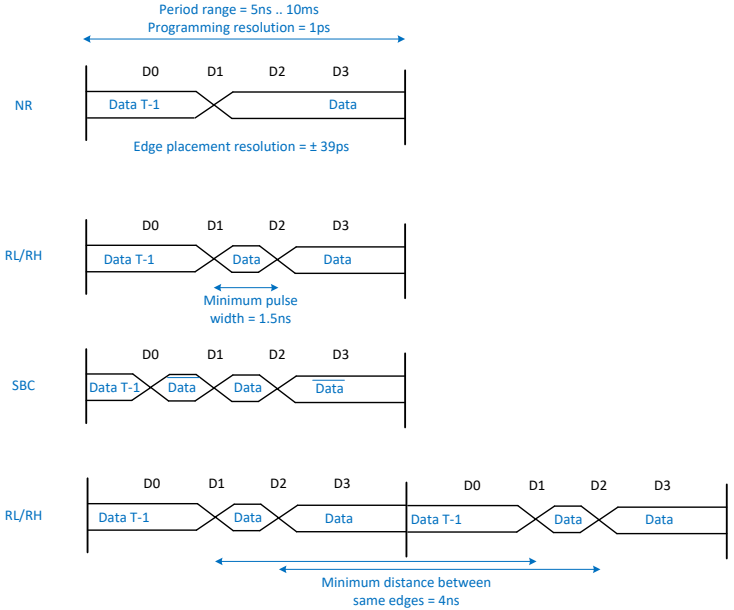
Implementations for ATE
and bench

-40V .. 110V
Linear supplies
Switching supplies

Cal resources
ADCs
High accurate measurement electronics (I, V)
Etc.

Multiple ATE interfaces.
Direct connection
Pogo solution
Cable solution

Drive formats (Flexible edge placement at 200MHz Vector)



Format	50Meps	100Meps	200Meps	400Meps	500Meps
NR	✓	✓	✓	×	×
RL	✓	✓	✓	✓	×
RH	✓	✓	✓	✓	×
SBL	✓	✓	✓	✓	✓
SBH	✓	✓	✓	✓	✓
SBC	✓	✓	✓	✓	✓

The xx Meps represents the number of events per second.

SALLAND Engineering
Test Technology Center

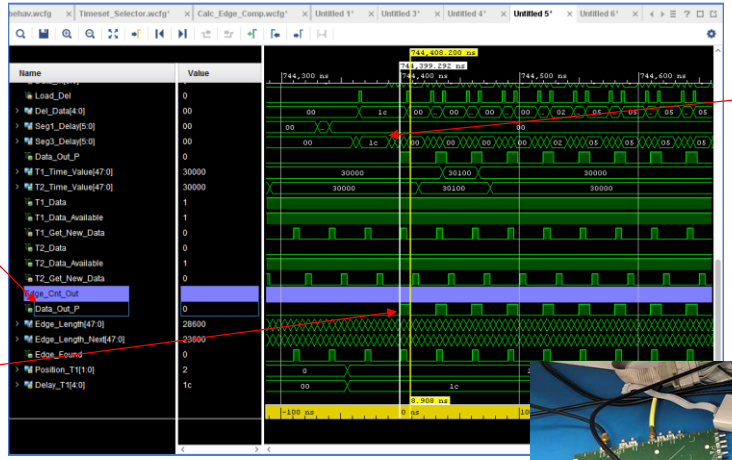
Development steps

For FPGA based Timing Generator/Pattern Generator

SALLAND Engineering
Test Technology Center

POC Timing Generator

Waveform example of shown concept



Output

Programmed pulse of 8.9ns.

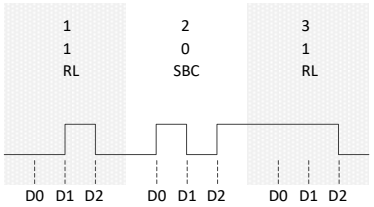
Programmed delay is 0x1C =28. This is 28*39ps = 1.092ns.

Period width = 10ns – 1.092ns = 8.908ns.

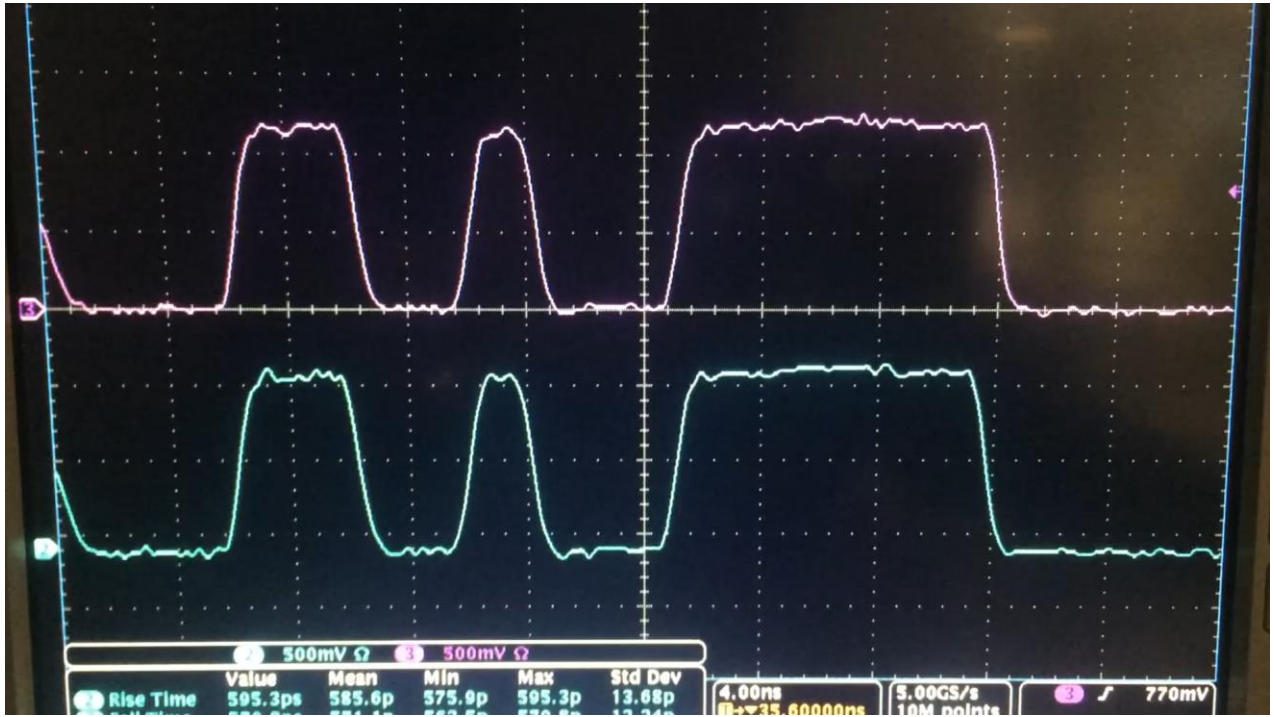
➔ Reason 8ps error

Driver signal EVM hardware

Vector	1	2	3
Data	1	0	1
Drive	RL	SBC	RL



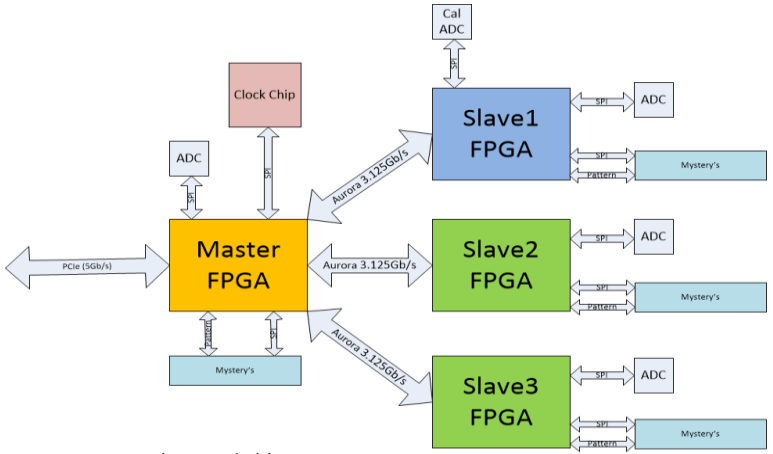
Moving edge 39 PS



Channel PoC results

- Pattern generation PoC
  - Based on a Mystery EVM and a FPGA Evaluation board
  - Generated waveforms with a pattern-rate of 200MHz on eight channels.
- The different waveforms are made with FPGA timing generator
  - RL,RH,NR,SBC, …
- Edge placement on the fly
  - Resolution of 39ps.
- The next step
  - Create a Reference Design with 64 channels on a 100x120mm PXIe board.

DPIN Architecture



Hardware

- Scalable architecture
- Blocks of 16 channels (1 FPGA, 2 Mystery's, ADC and Memory (12Gb))
- Boards with 1..4 blocks
- Multiple Boards in a rack

Timing generation

- Every edge is generated using a jitter-free 400MHz clock.
- The pattern Sequencer/Timing generator is running at 200MHz.

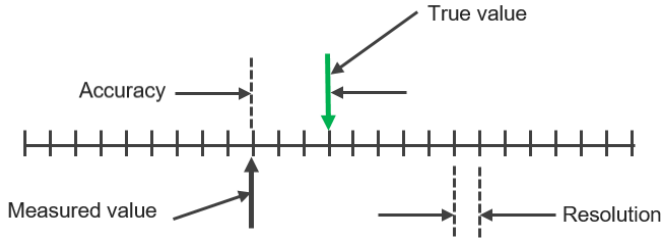
Synchronization

- One board, local synchronization signals
- Multiple boards, Synchronization signals over backplane to Synchronize boards

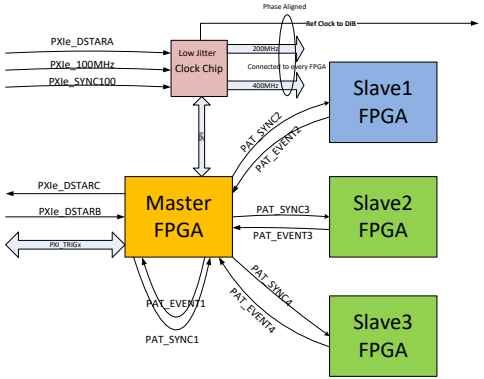
Target Timing specification

- Edge Placement Accuracy Drive ±250ps
- Edge Placement Accuracy Compare ±500ps
- Pin-to-Pin skew ±500ps
- Resolution 39ps

Accuracy is how close a reported measurement/setting is to the true value.
Resolution is the smallest step/change that can be measured/set.



Synchronization



On board pattern sequencer synchronization

- Synchronization lines to each blocks
- Data Communication between blocks is done using an Aurora Bus.

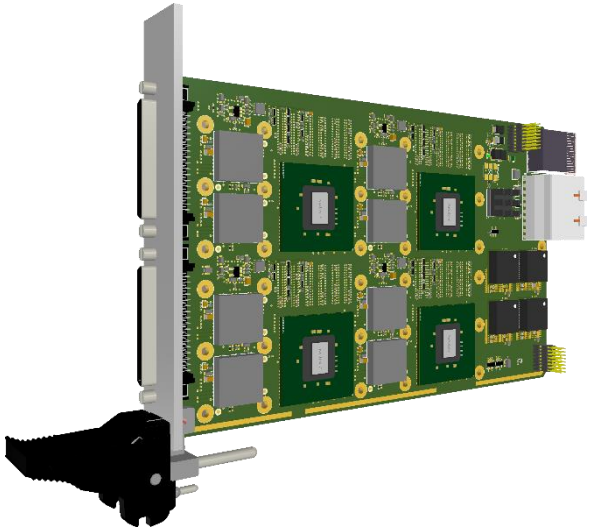
Board to board pattern sequencer synchronization

- Synchronization lines to each board on backplane
- Data Communication between boards is done using a PCIe bus.

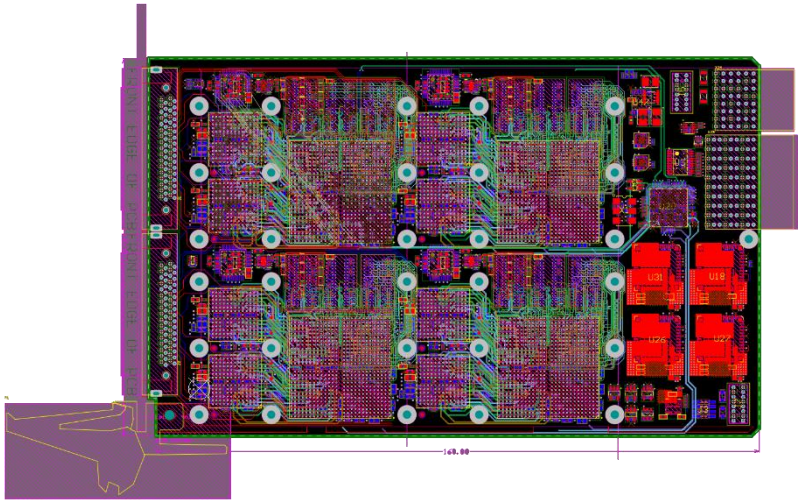
Pass/Fail information

- Conditional statement information in pattern sequencer are shared via backplane to each block

Reference design, PXIe IO Channel card



64ch, max 200MHz flexible edge placement



Dimensions: 100mm*160mm