Low Energy Design Techniques for Data Converters

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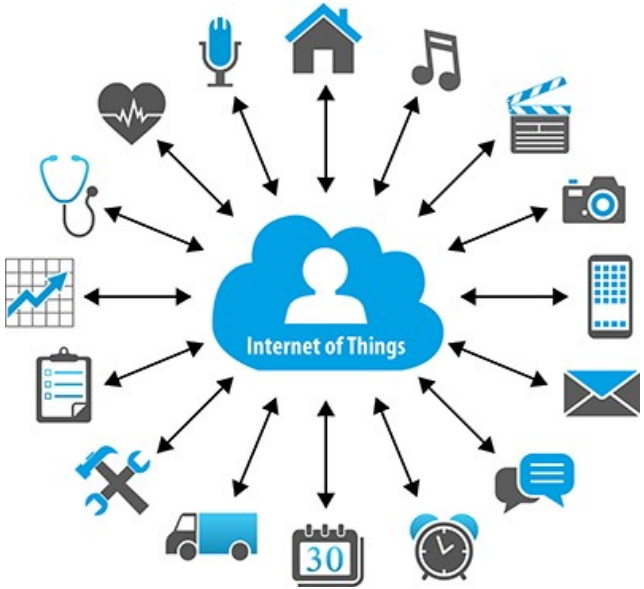
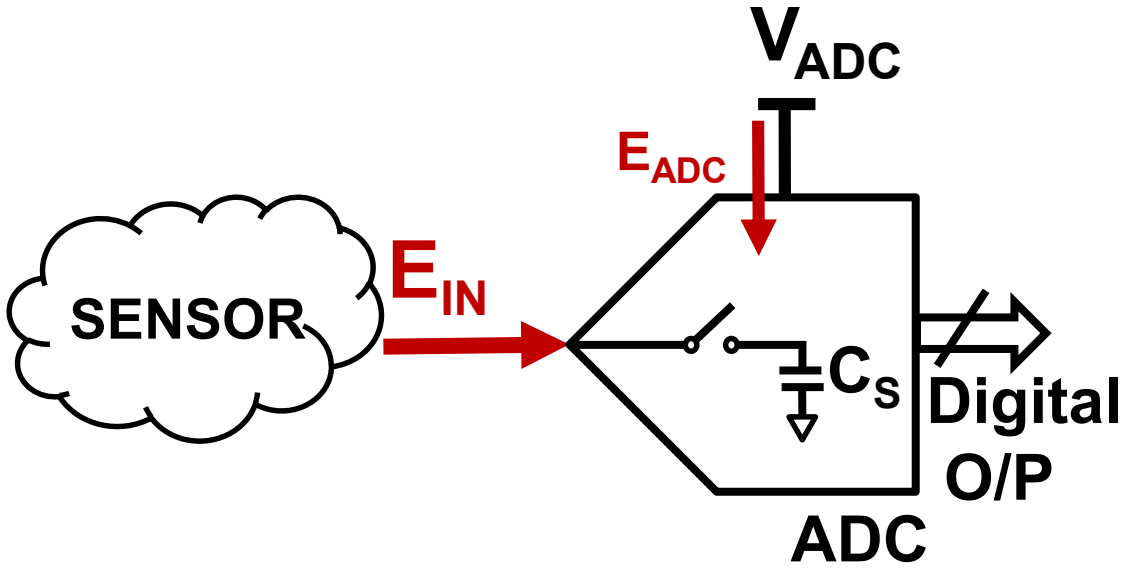
Overview

- Motivation
  - Input Buffer Requirement
- Reducing Input Drive Current
- Low power single supply buffered SAR ADC
  - Proposed Solution
  - Integration of Buffer with SAR ADC
  - Offset Correction
- Measurement Results
- Conclusion

Motivation





- Overall low energy (E_{IN}+ E_{ADC}) consumption

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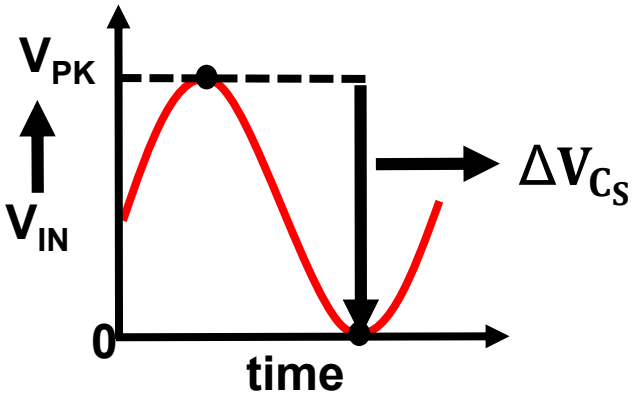
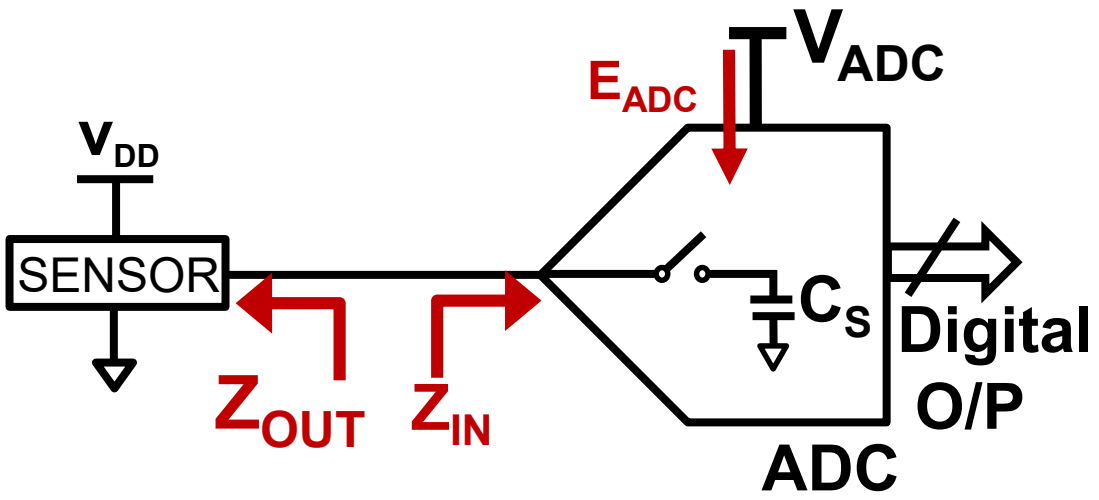
Motivation – Input Buffer



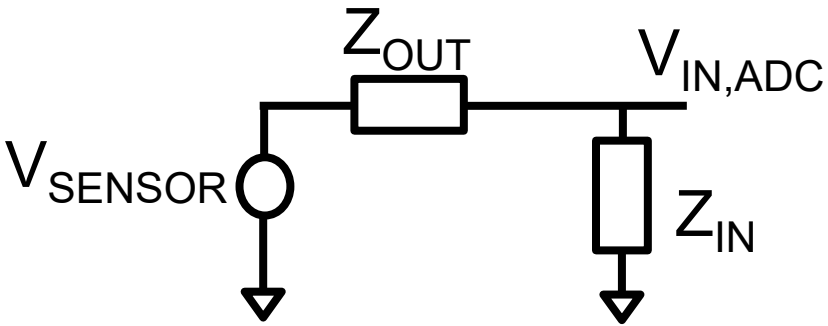


Low Power (V^2/Z_{OUT})

Low Noise (kT/C_S)
(Large C_S)

$$Z_{OUT} > Z_{IN}$$

Motivation – Input Buffer



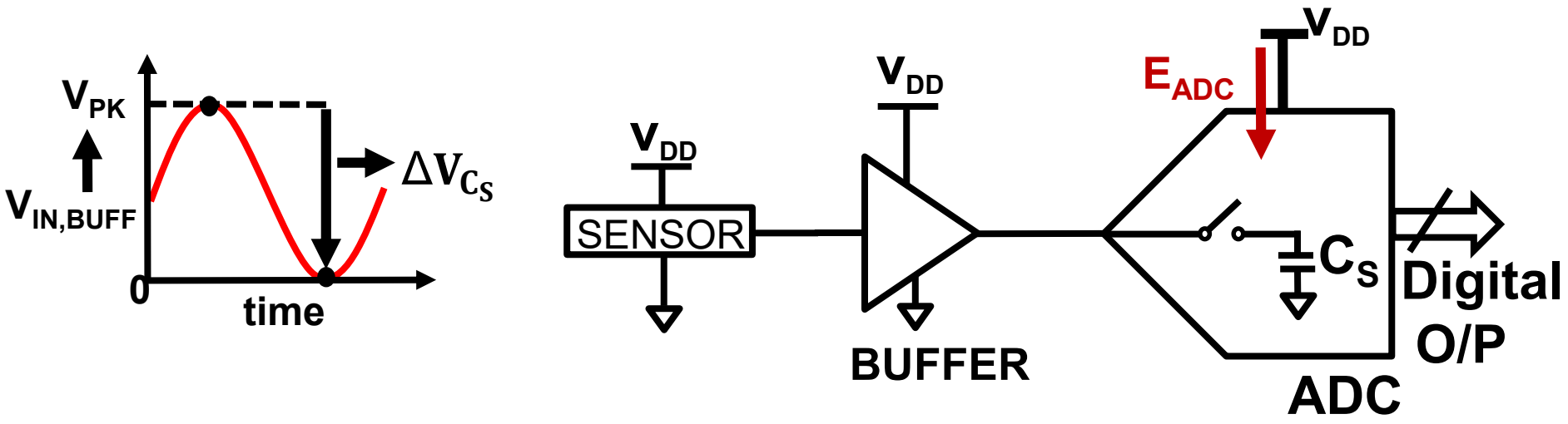
$$V_{IN,ADC} = \frac{Z_{IN}}{Z_{IN} + Z_{OUT}} V_{SENSOR}$$

$$\mathbf{Z_{OUT} >> Z_{IN}}$$

$$\mathbf{V_{IN,ADC} \approx 0}$$

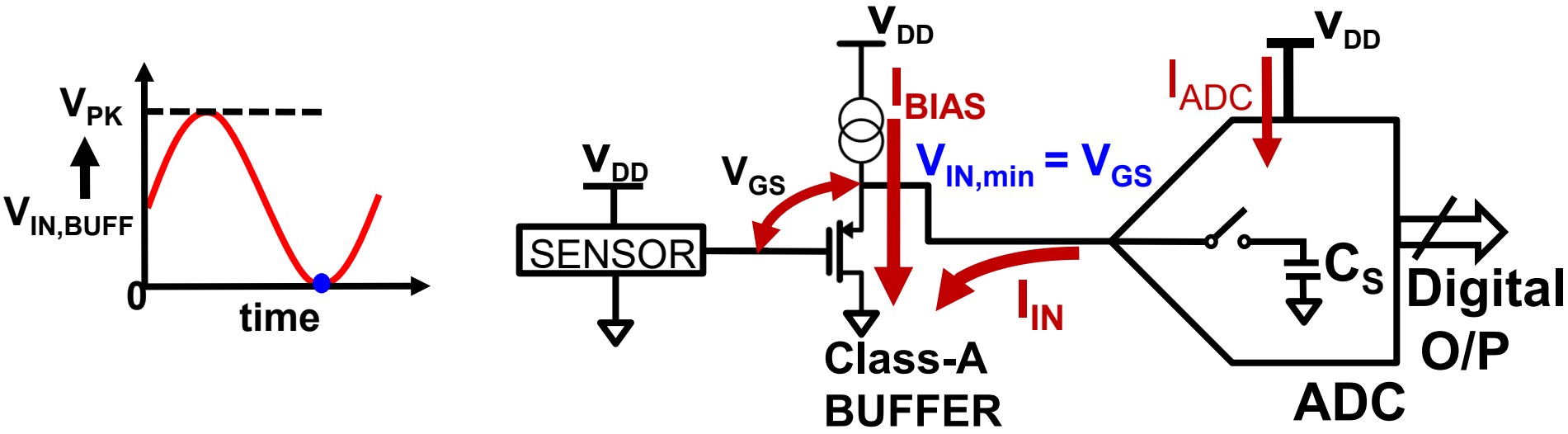
Low power sensor cannot drive ADC input

Motivation – Input Buffer



Buffer the input signal !!

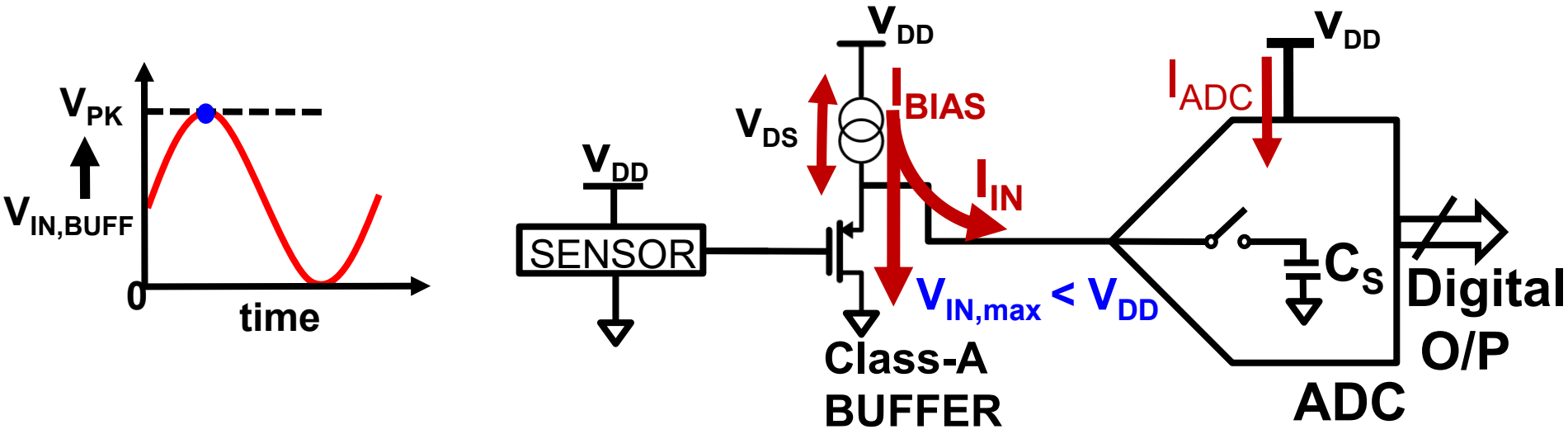
Motivation – Input Buffer Requirement



☺ Class-A buffer : low distortion, always “ON” output stage.

☹ $V_{IN,min} > V_{GS}$. Rail-to-rail operation not feasible with single supply.

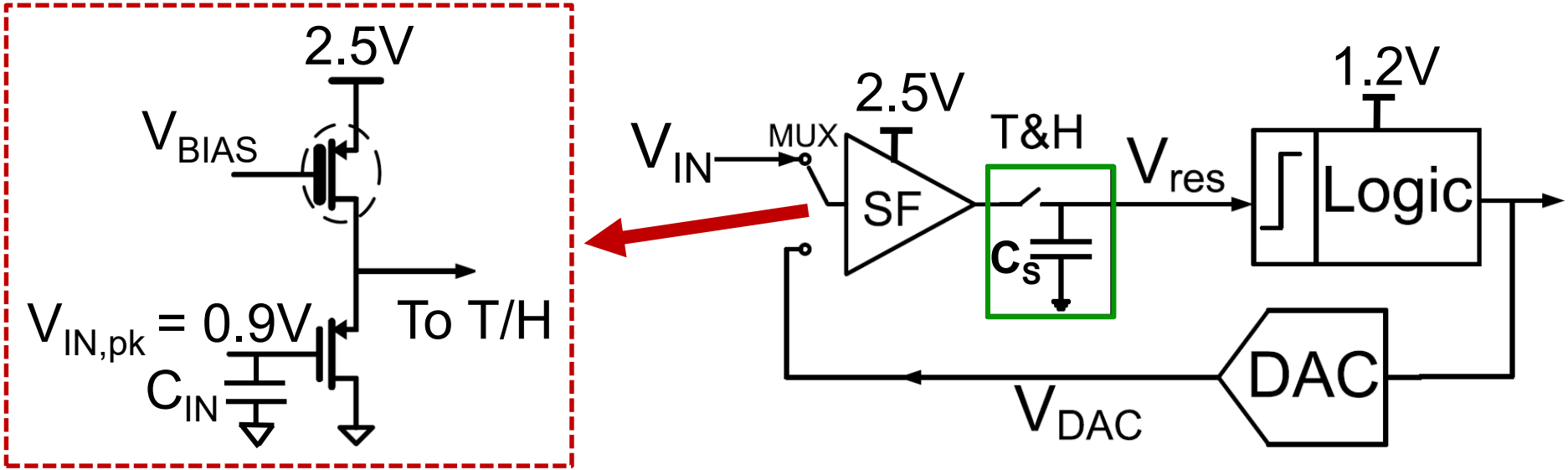
Motivation – Input Buffer Requirement



☹ $I_{BIAS} \geq I_{IN,MAX}$ and $V_{IN,max} < V_{DD} - V_{DS}$

☹ Power hungry and poor efficiency. $P_{BUFF} \geq V_{PK} I_{BIAS}$

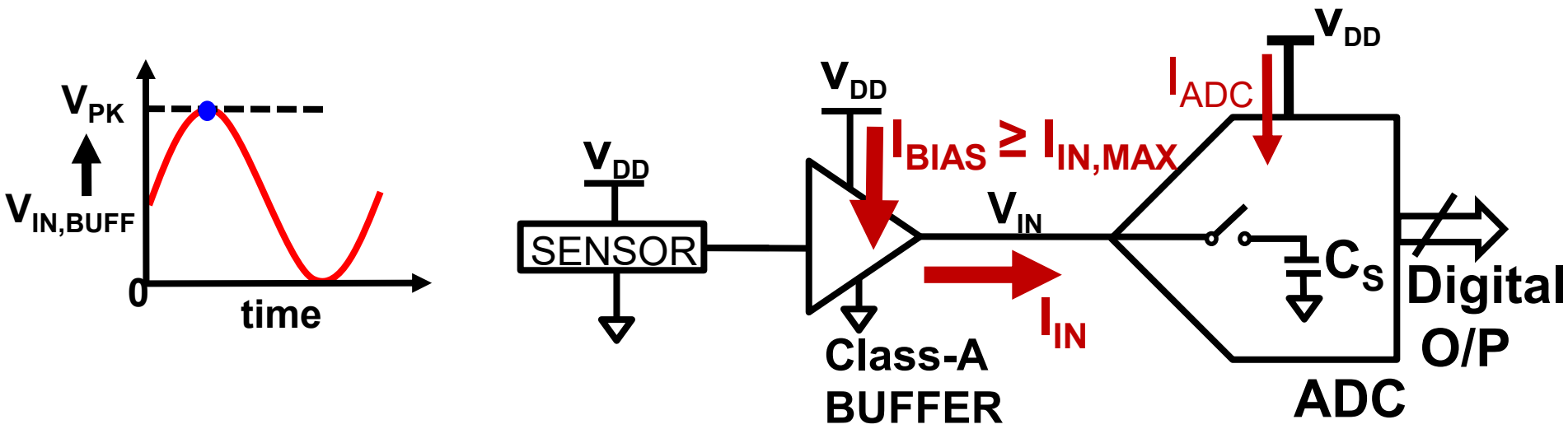
Prior Art - Source Follower embedded in SAR



- ☺ Input capacitance (C_{IN}) is 0.2pF (18x lower than C_S)
- ☹ Additional high supply voltages (≈ 3xV_{PK}) required

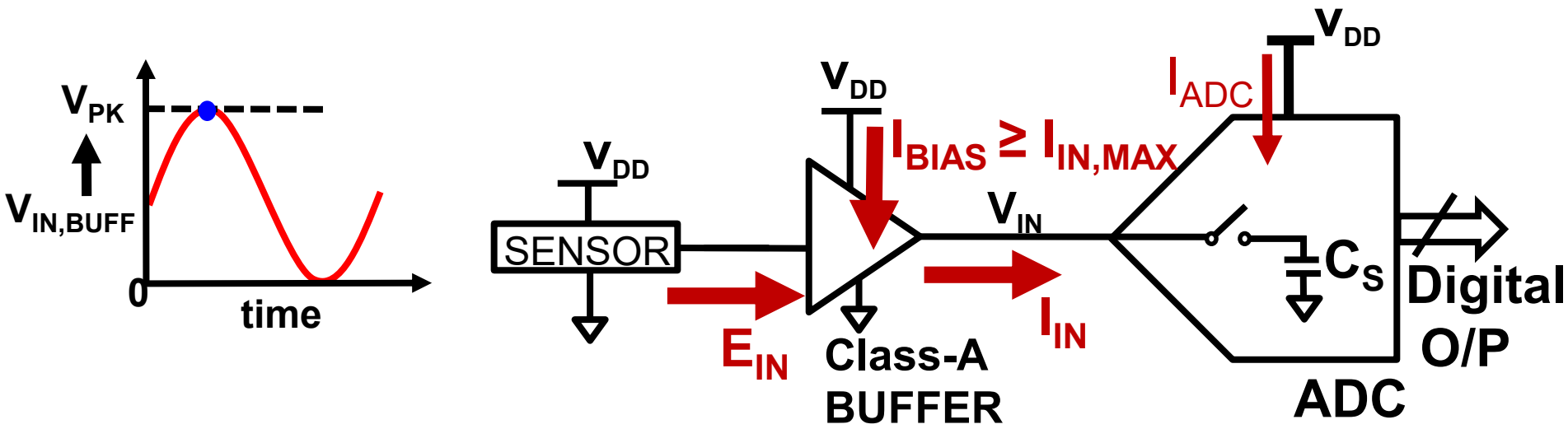
Krämer, *JSSC* 2015

Motivation – Input Buffer Requirement



- Walden FoM (incl. buffer), $FoM_{W,buff} = (P_{ADC}+P_{BUFF})/(f_S \cdot 2^{ENOB})$
- **P_{BUFF} ⇧ → $FoM_{W,buff}$ ⇧**

Motivation – Input Buffer Requirement



- Single V_{DD} with near rail-to-rail signal swing.
- Minimize I_{BIAS} (or $I_{IN,MAX}$) → low $FoM_{W,buff}$.
- Minimize E_{IN}.

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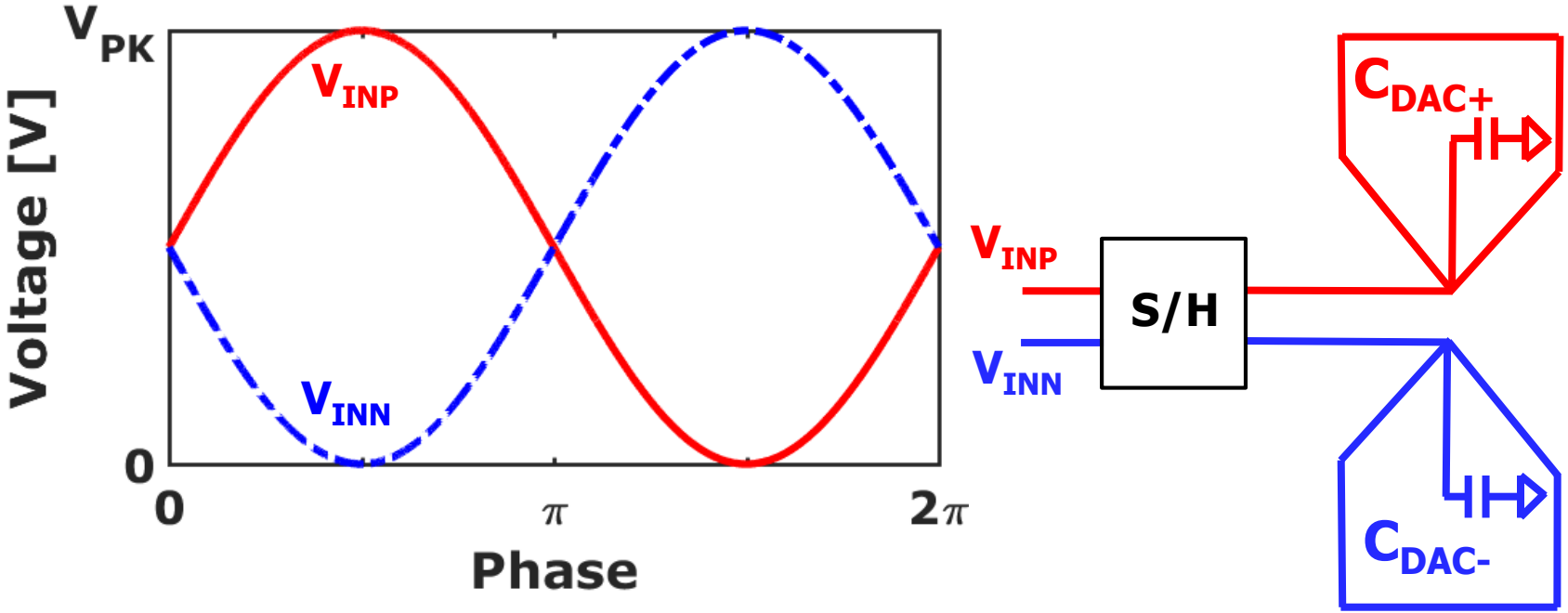
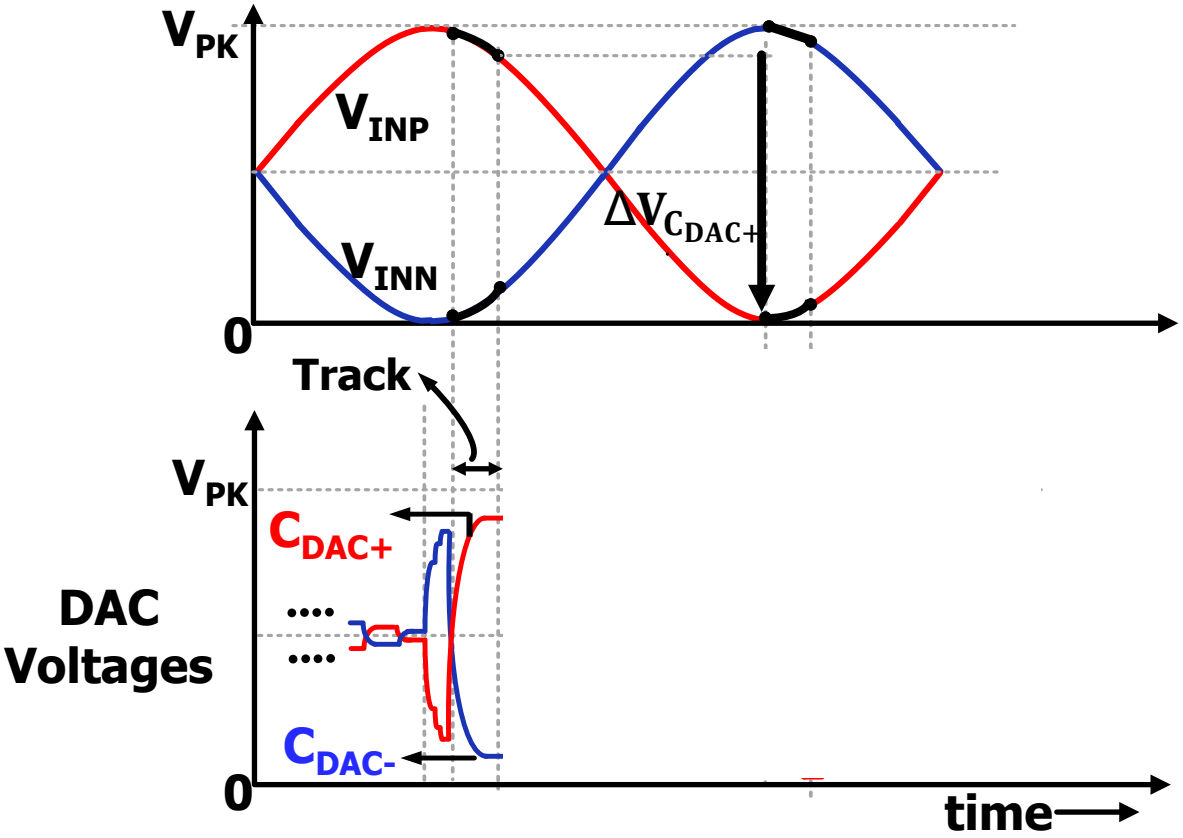
Conventional

- V_{INP} sampled on C_{DAC+}

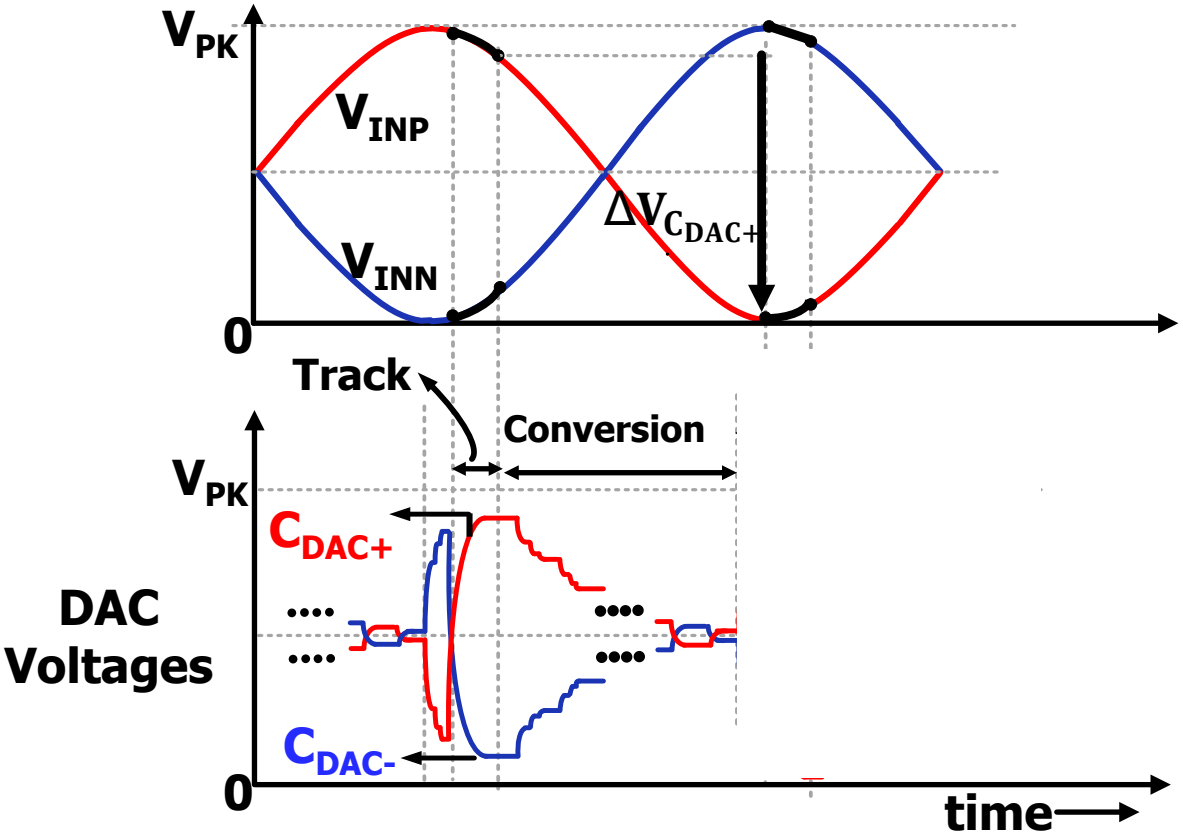


- V_{INN} sampled on C_{DAC-}
- Peak Sampling current, $I_{PK} = V_{PK}/R_{SH}$

Conventional



Conventional



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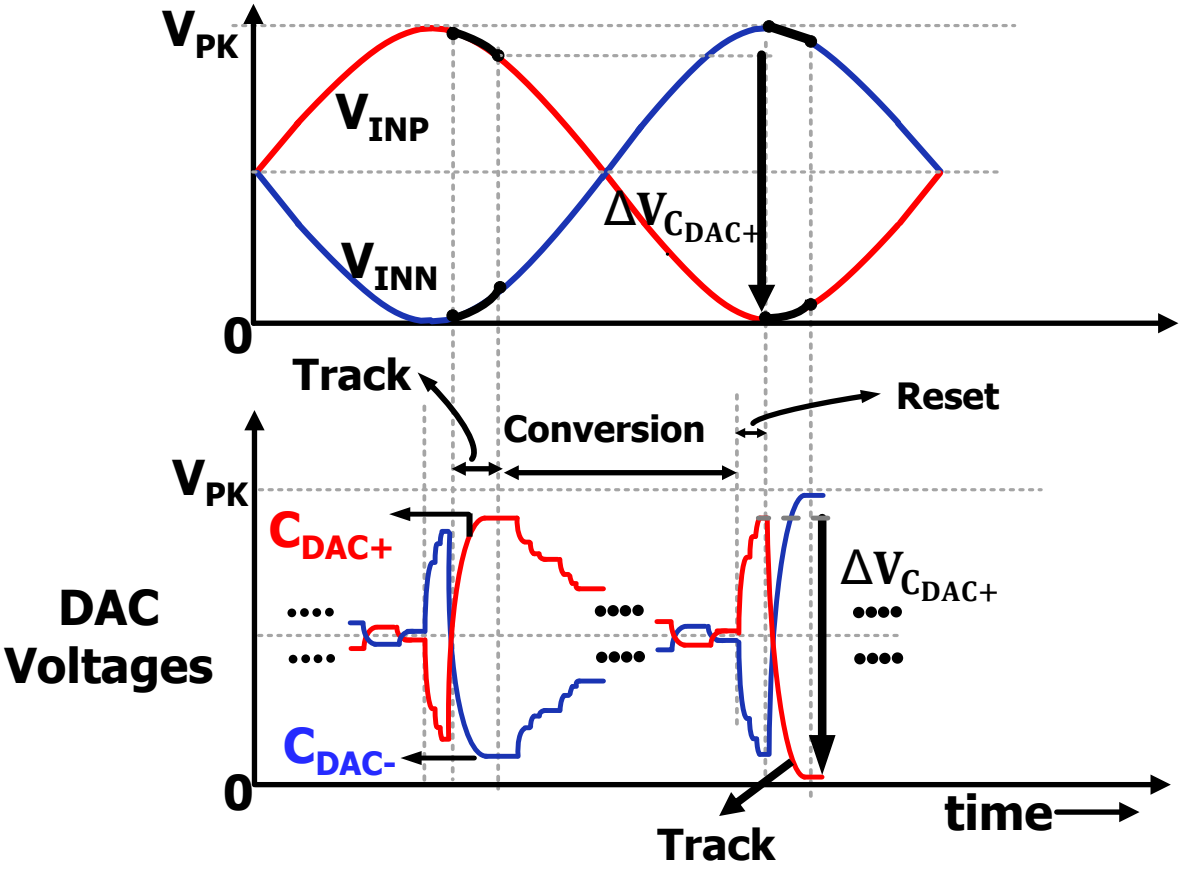
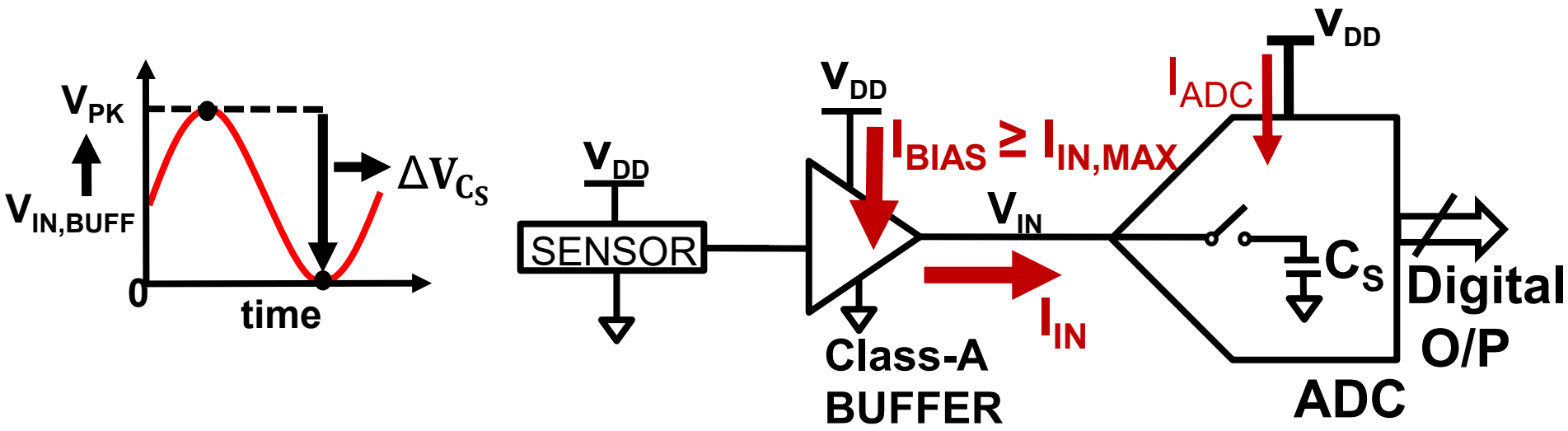
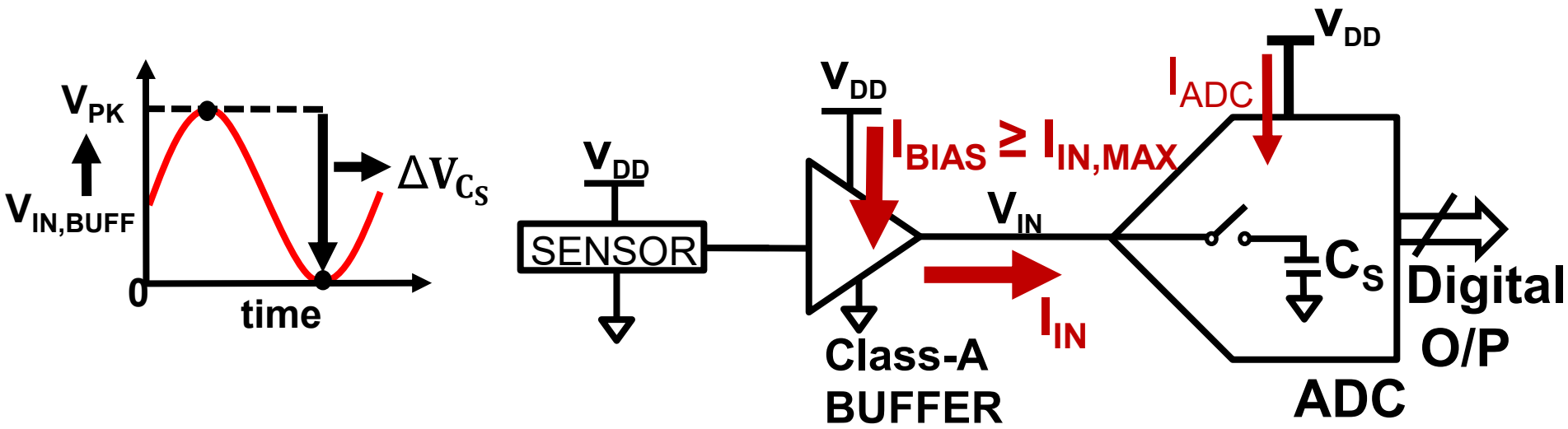


Reducing ΔV_{C_S} and Input Current



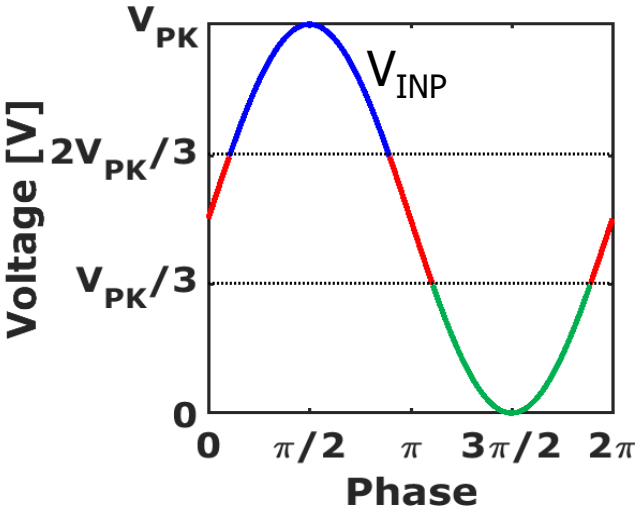
- For Nyquist rate ADCs, $\Delta V_{C_S} \leqslant V_{PK}$
- $I_{IN,MAX} = (N \cdot C_S \cdot V_{PK}/T_{TRACK})$ [N = 0.69(#Bits)]

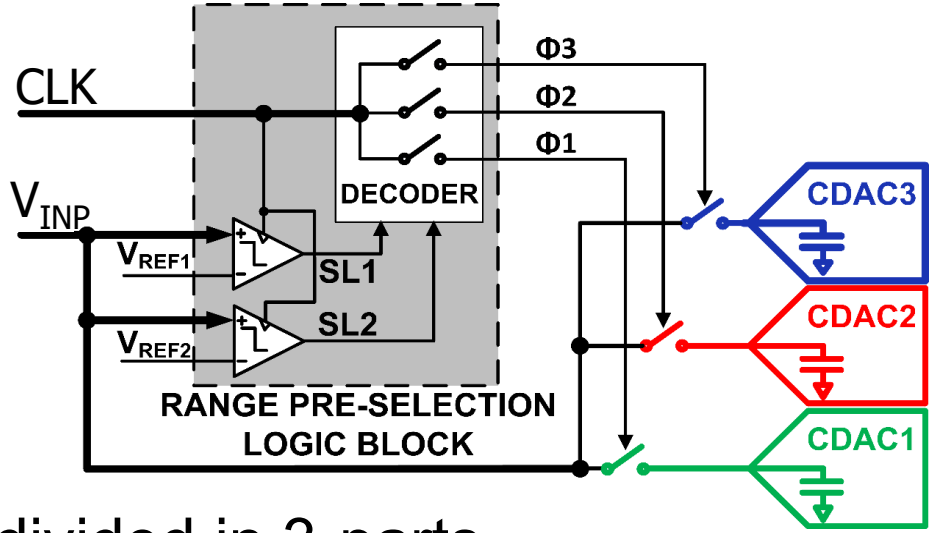
Reducing ΔV_{C_S} and Input Current



- Linear Settling
  - $I_{IN,MAX} = (N \cdot C_S \cdot \Delta V_{C_S} / T_{TRACK})$
- $I_{IN,MAX}$ ⇩ → ΔV_{C_S} ⇩

Reducing ΔV_{C_S} and Input Current

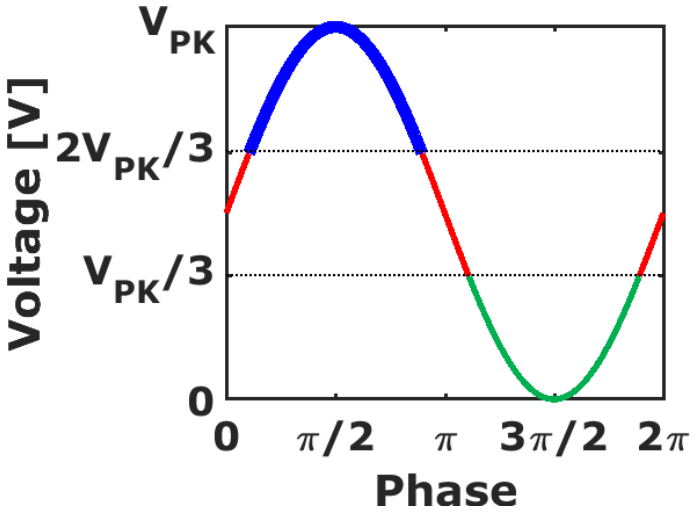


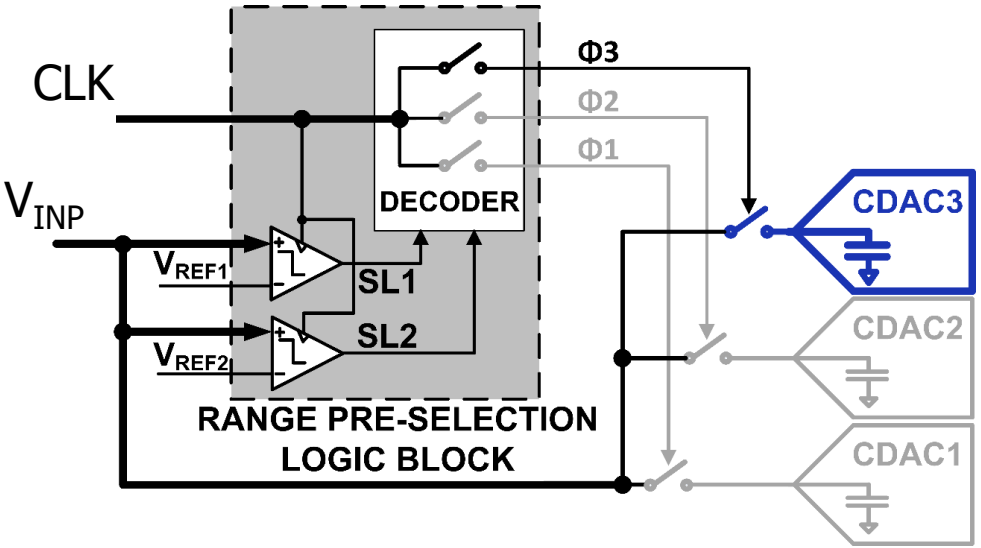


- Full-scale range of V_{INP} divided in 3-parts
  - Each sub-range of V_{INP} sampled onto the respective CDAC
  - Limits the ΔV_{C_S} to $V_{PK}/3$

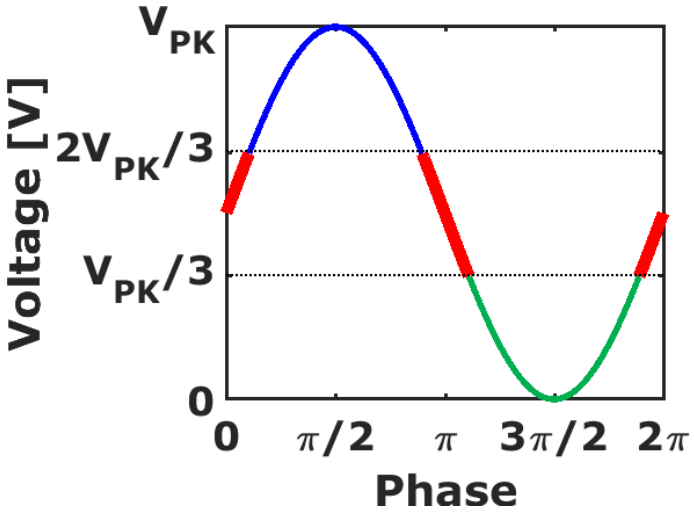
[Bindra, *ASSCC 2017*]

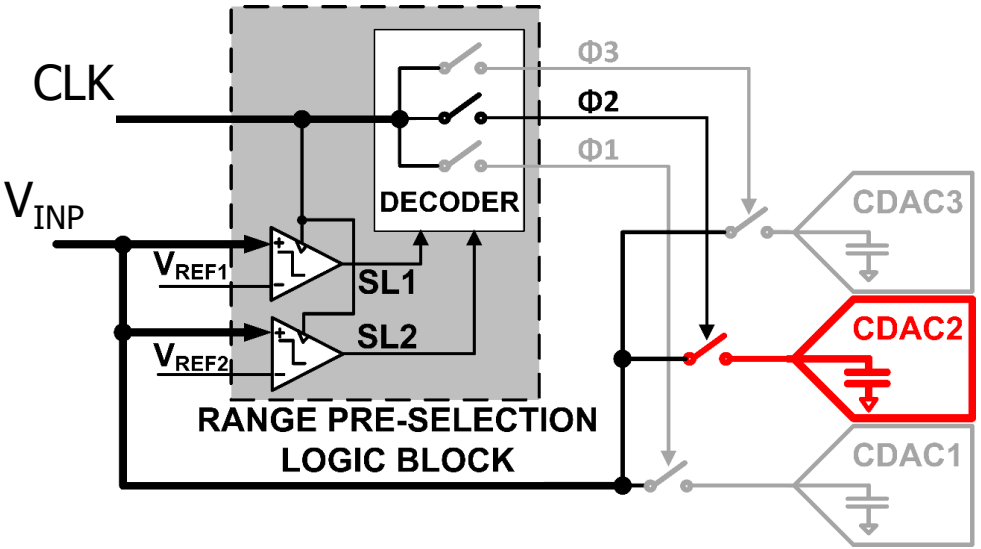
Reducing ΔV_{C_s} and Input Current



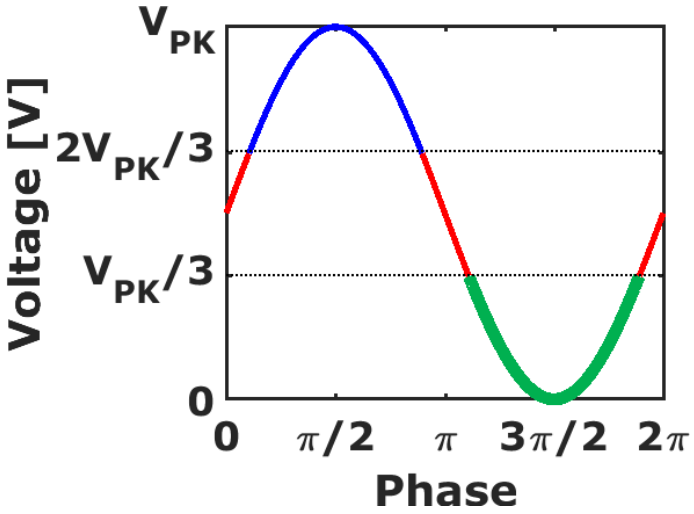


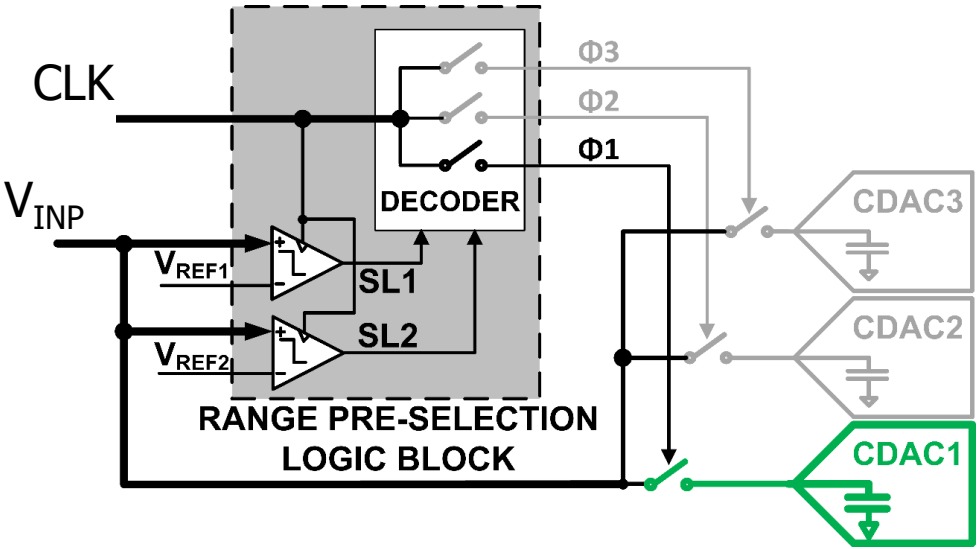
Reducing ΔV_{C_s} and Input Current



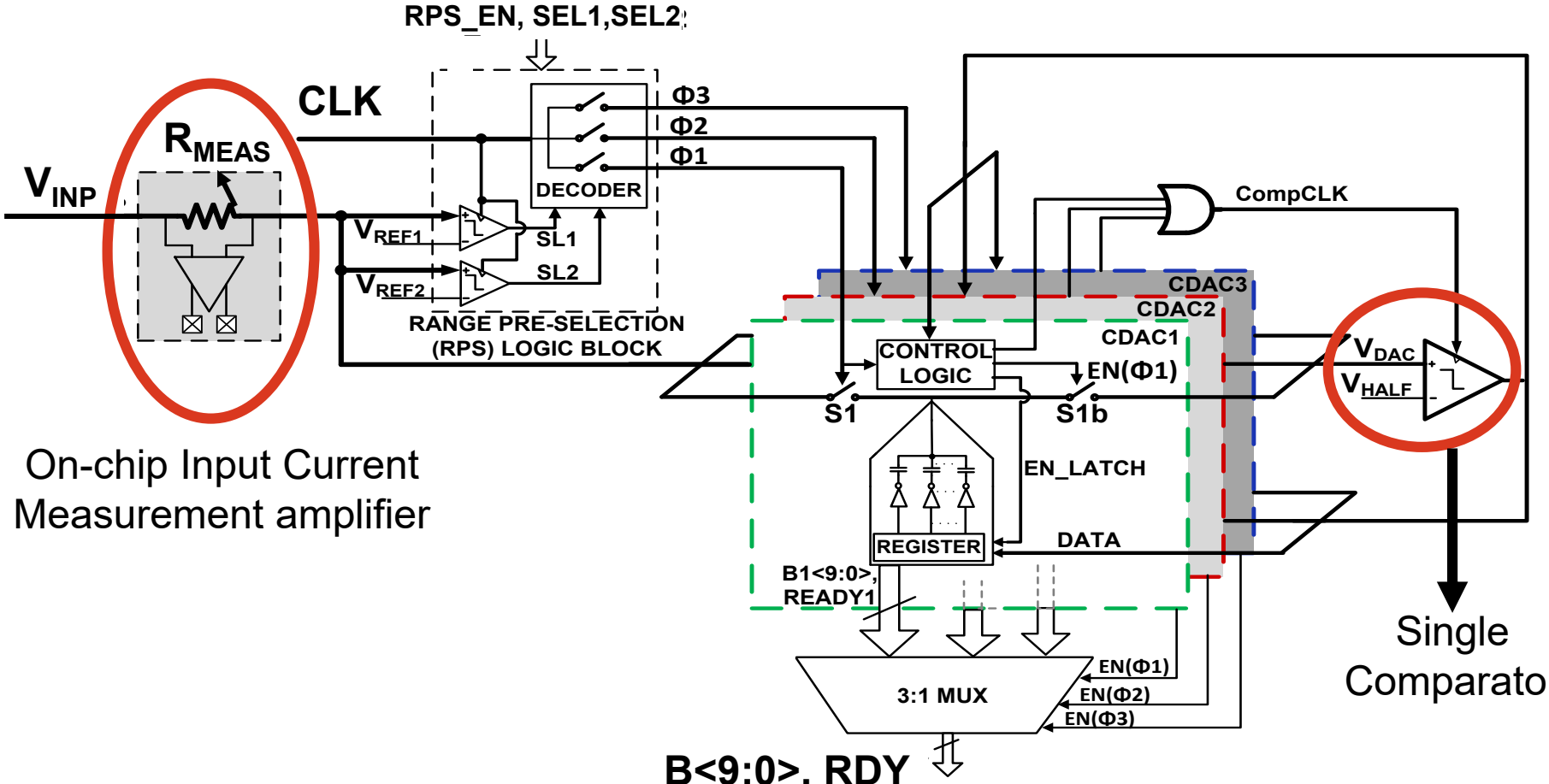


Reducing ΔV_{C_S} and Input Current



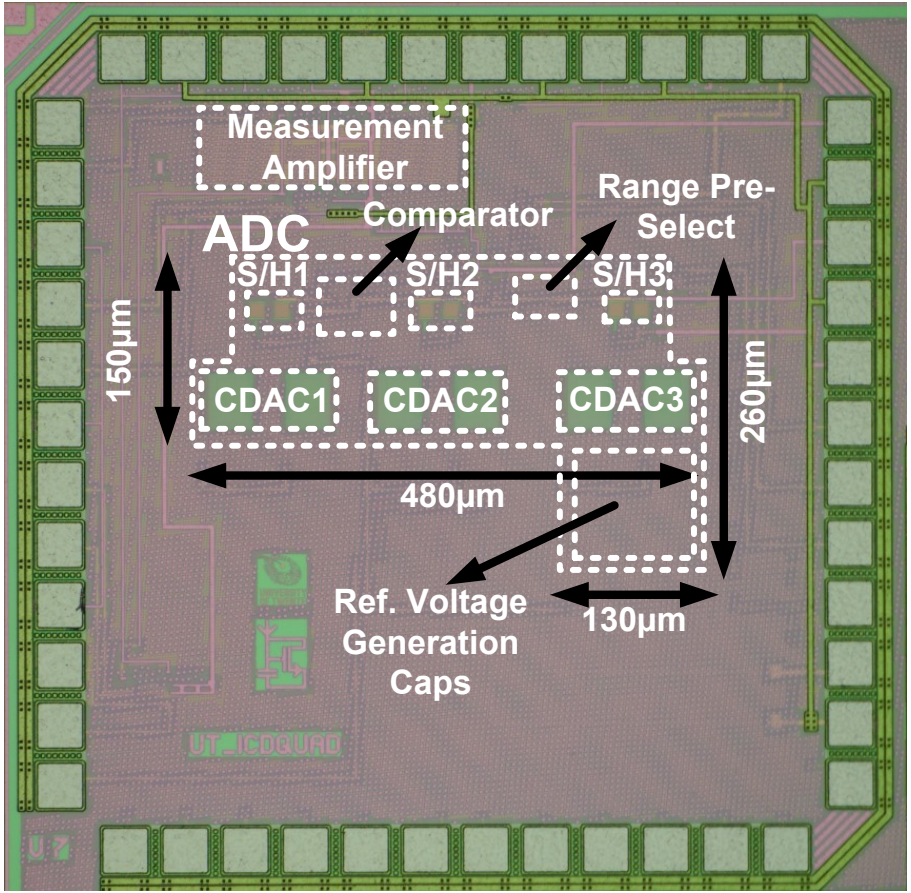


Measurement - Input Sampling Current



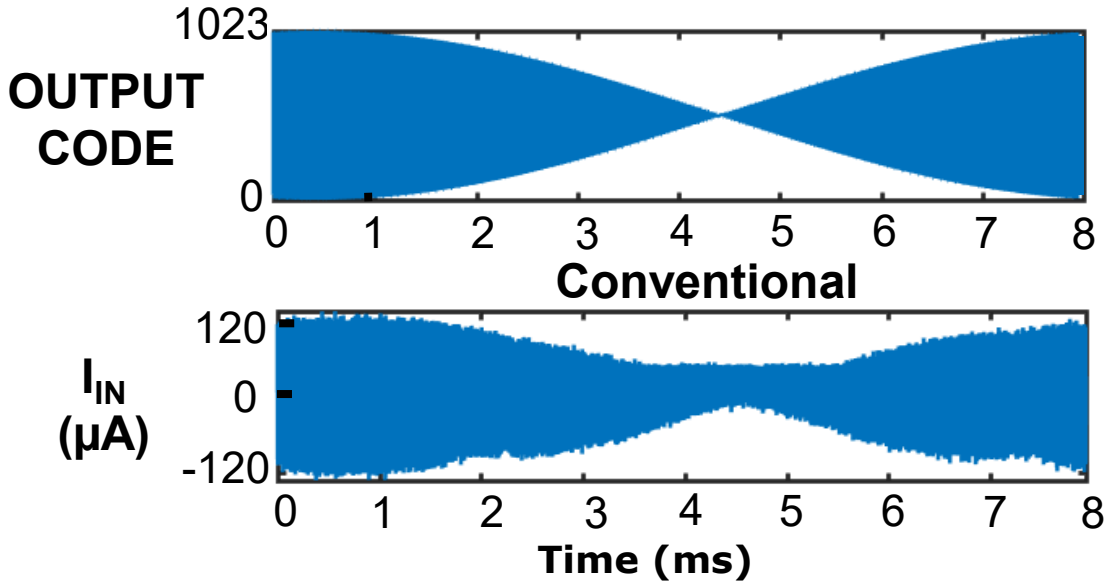
On-chip Input Current
Measurement amplifier

Die micrograph (65nm CMOS)



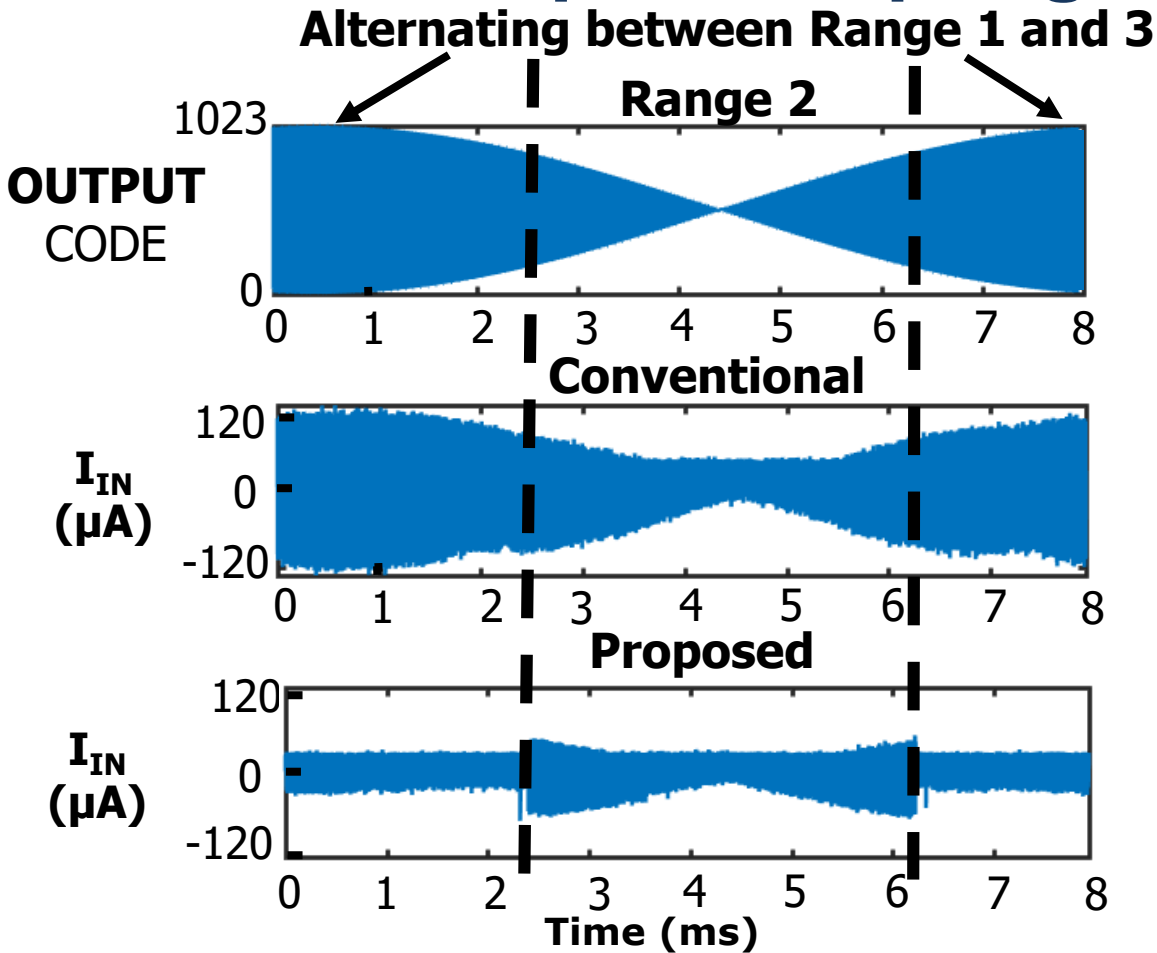
- Area – 0.08 mm^2 (including decaps)
- Measurement amplifier to compare input sampling current
- CDACs not selected act as decap (connected to single reference voltage)

Measurements- Input Sampling Current

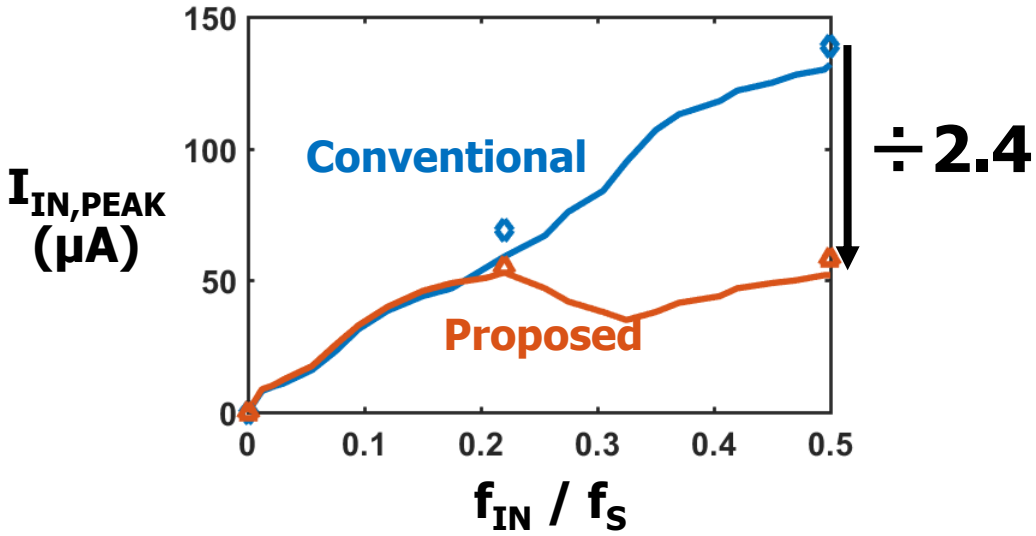


- f_S = 2MS/s and f_{IN} = 999.9375kHz
- Beat frequency = $f_S/2 - f_{IN}$ = 62.5 Hz
- $I_{IN} = \Delta V_{C_s} / (R_{MEAS} + R_{SH})$
- $R_{MEAS} + R_{SH} \leq 1/[(N+1) \cdot C \cdot 10 \cdot f_S]$

Measurements- Input Sampling Current



Reducing ΔV_{C_S} and Input Current



☺ Reduced ΔV_{C_S} reduces peak input sampling current.

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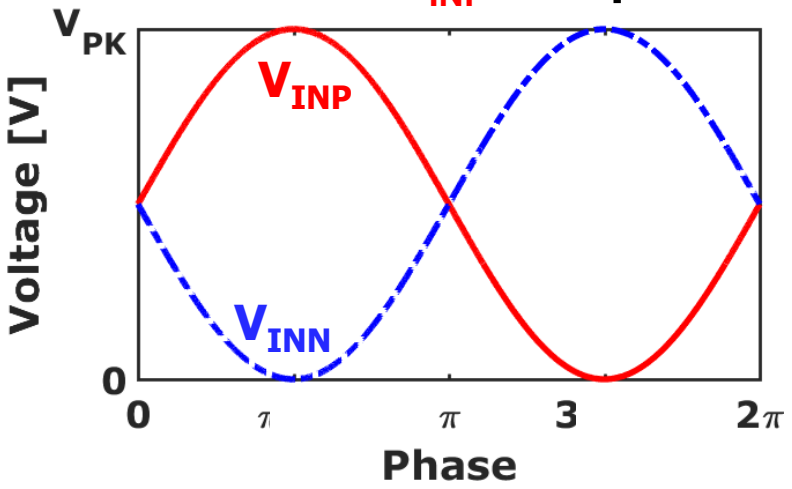
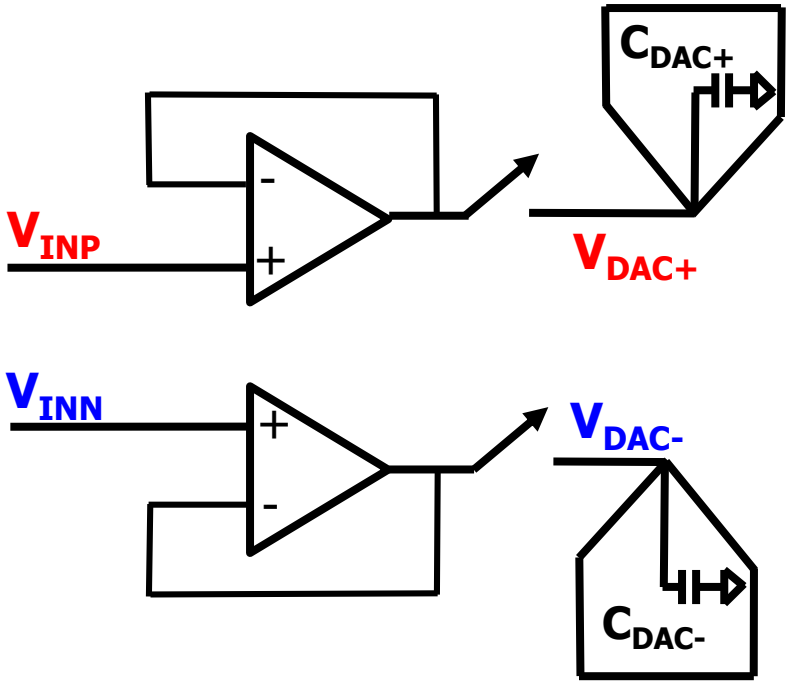
Conventional Architecture

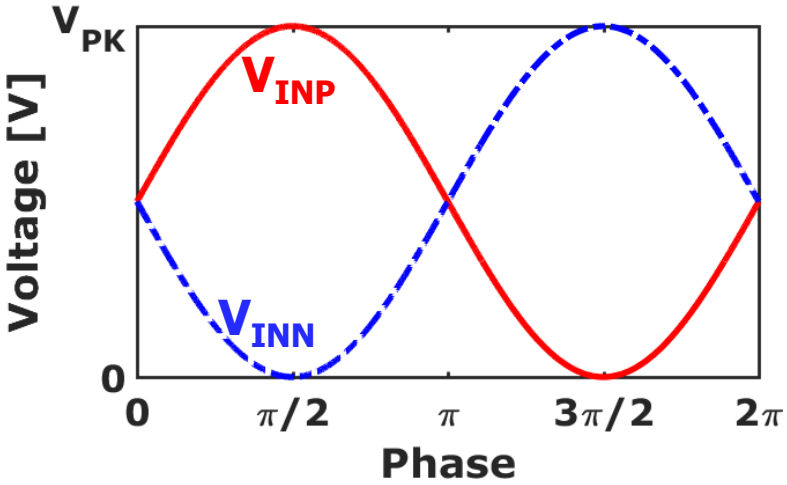
- V_{INP} sampled on C_{DAC+}

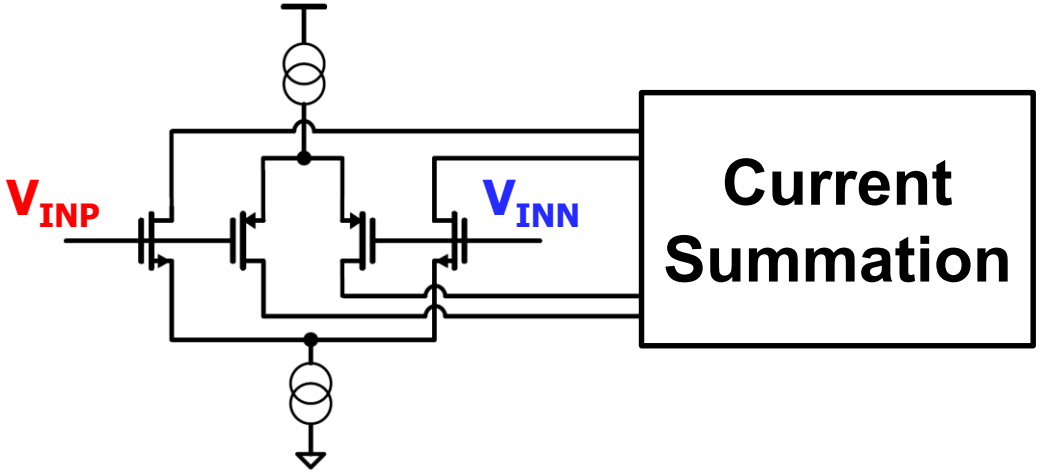


- V_{INN} sampled on C_{DAC-}



Conventional Architecture





☺ Complimentary input pair can handle rail-to-rail input.

☹ Distortion due to signal dependent gm variation and offset modulation.

[Huijsing, *JSSC 1980*]

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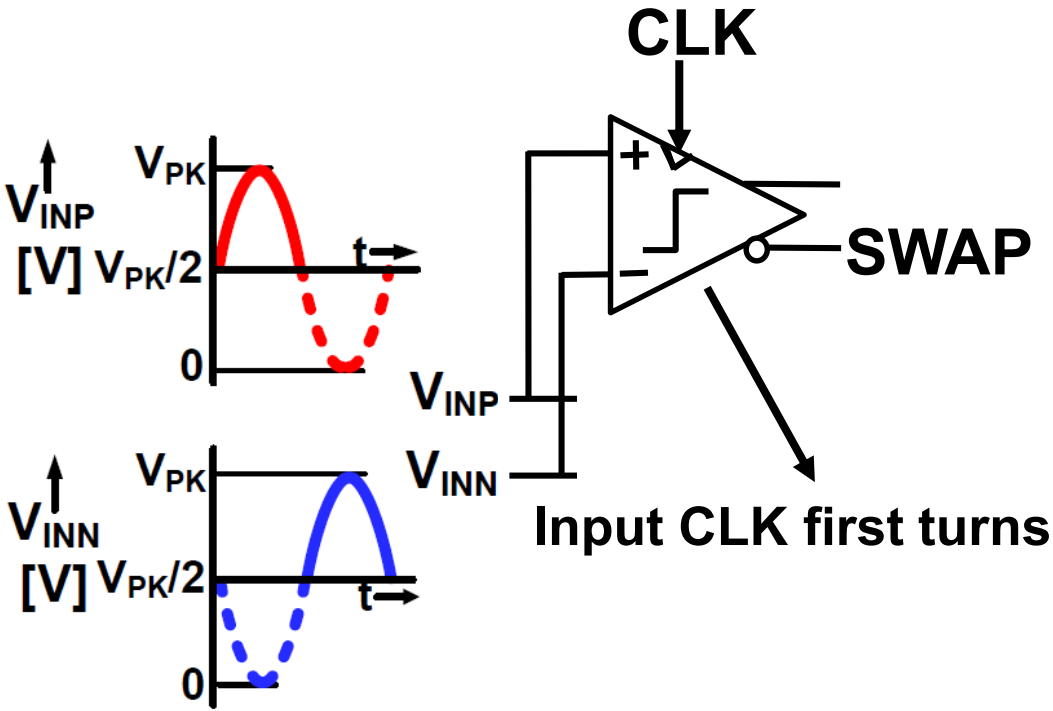
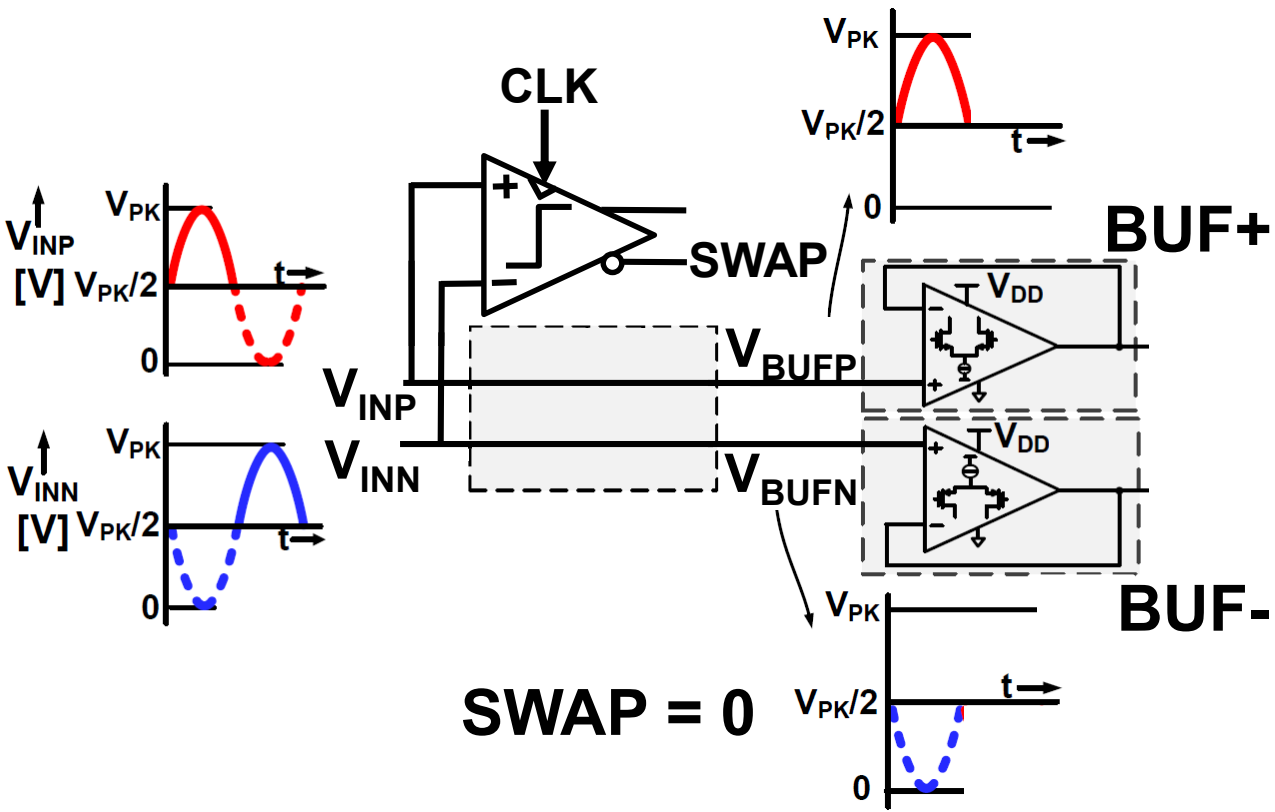
Architecture - Front End



Input CLK first turns ON the Front end comparator

[Bindra, *CICC 2019*]

Architecture - Front End



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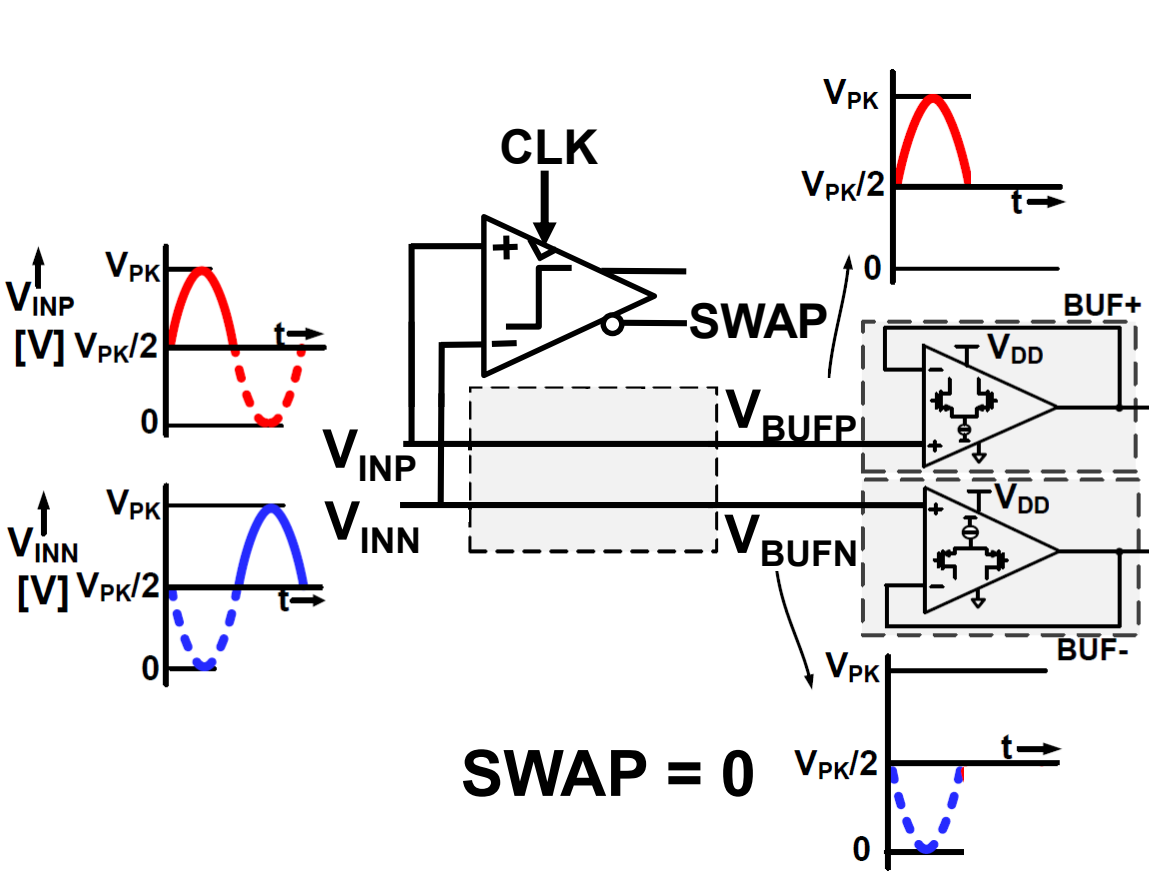

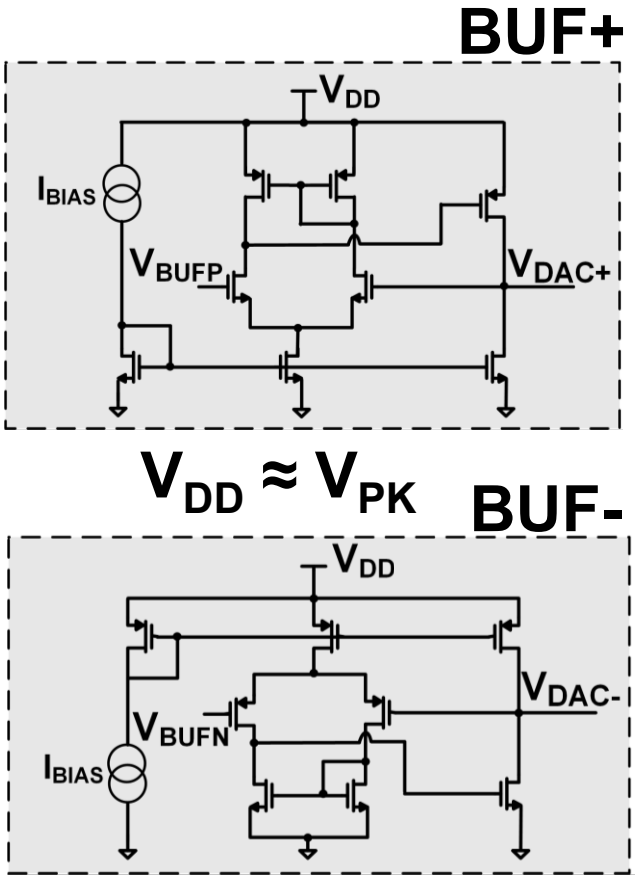

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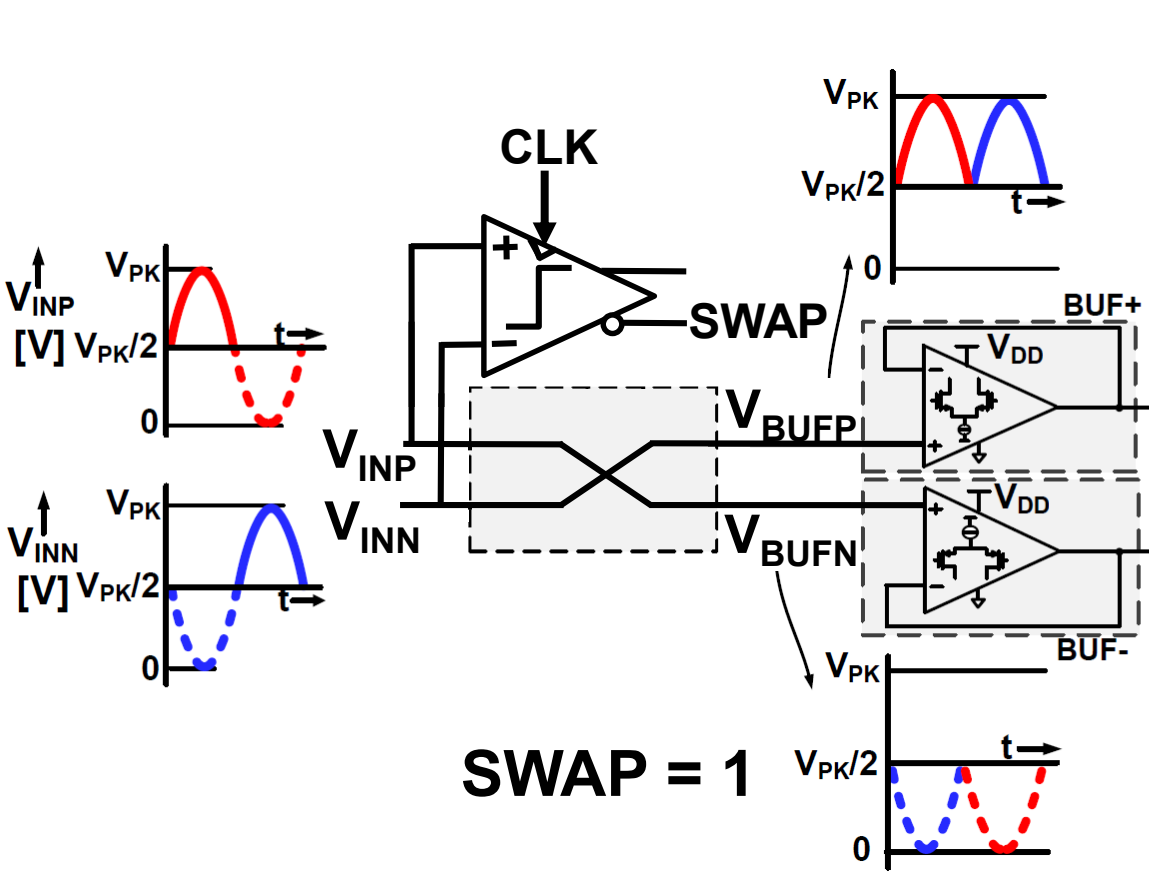

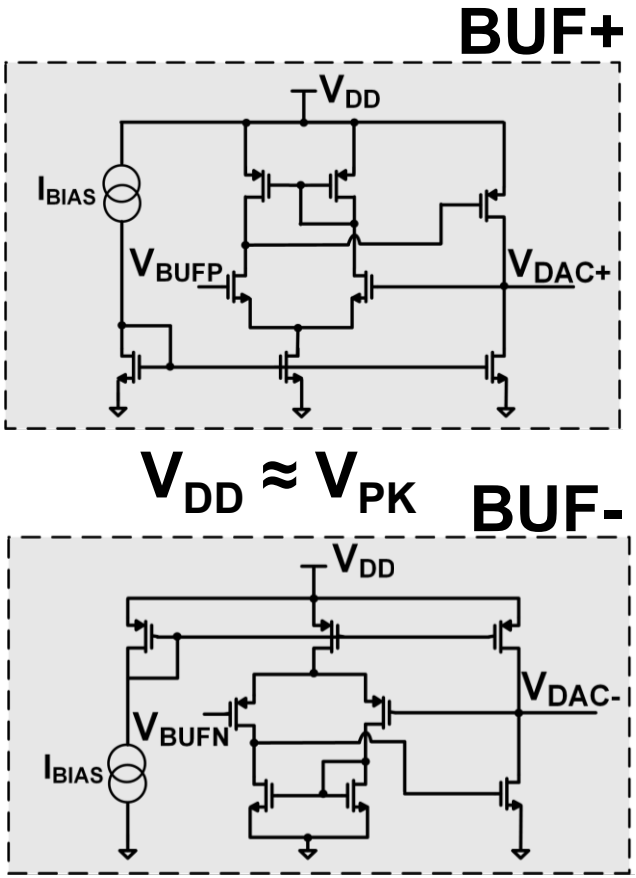

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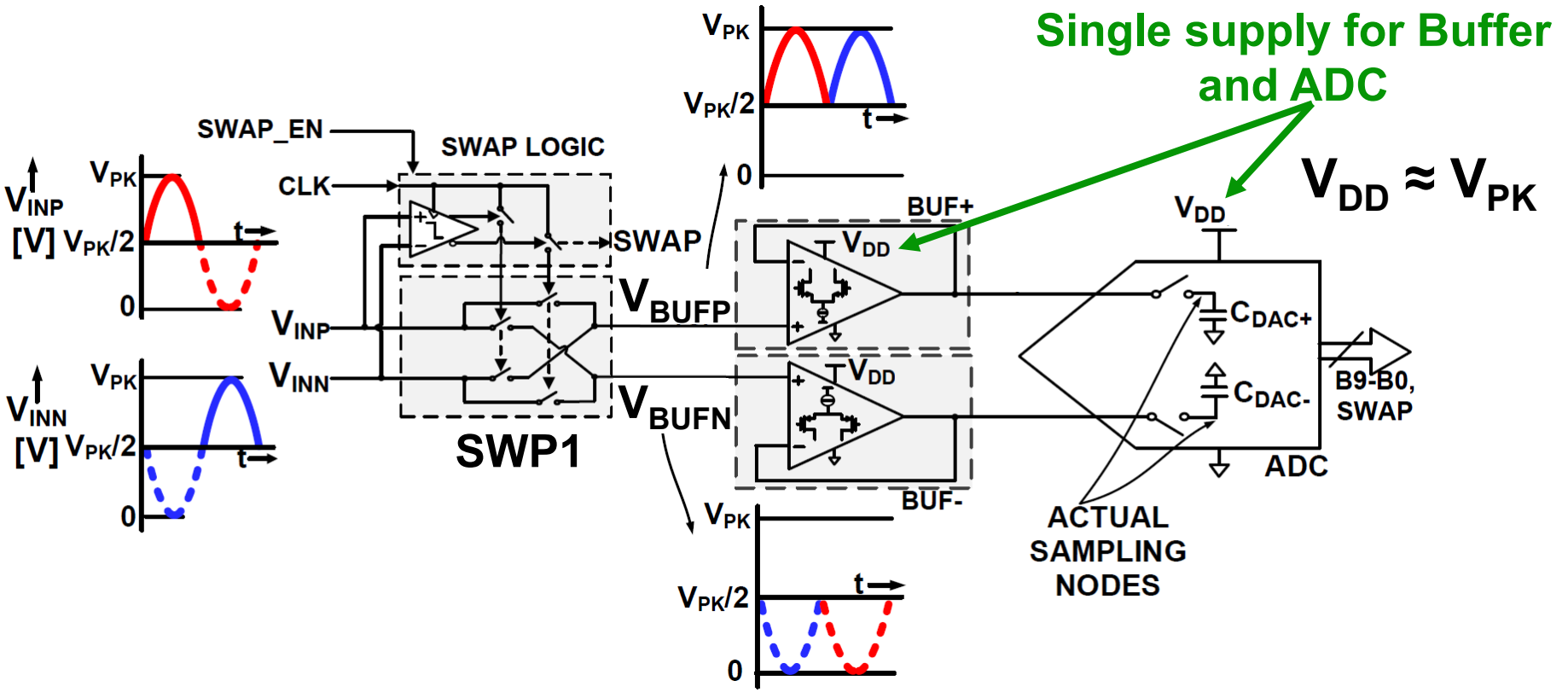

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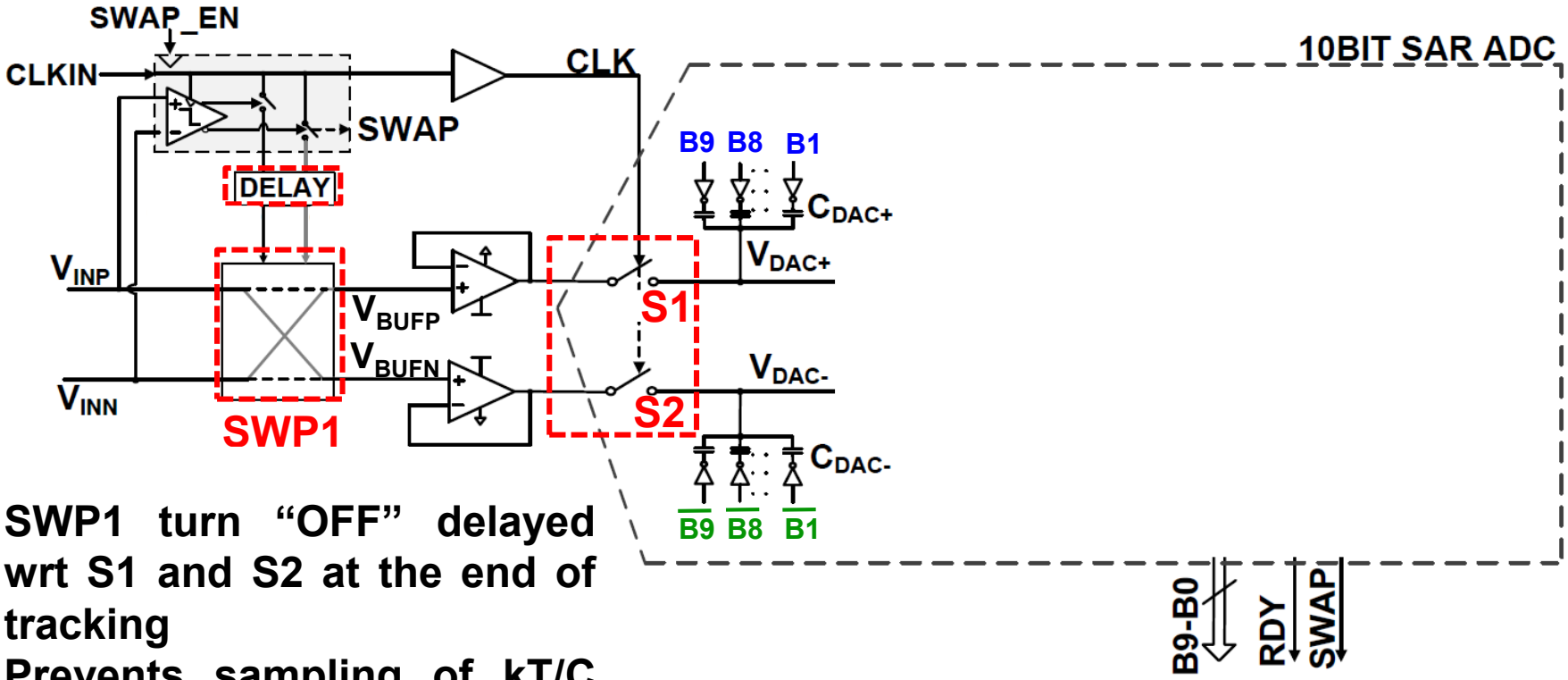
Architecture - Buffers integrated with ADC



- SWP1 turn "OFF" delayed wrt S1 and S2 at the end of tracking
- Prevents sampling of kT/C noise at the buffer's input

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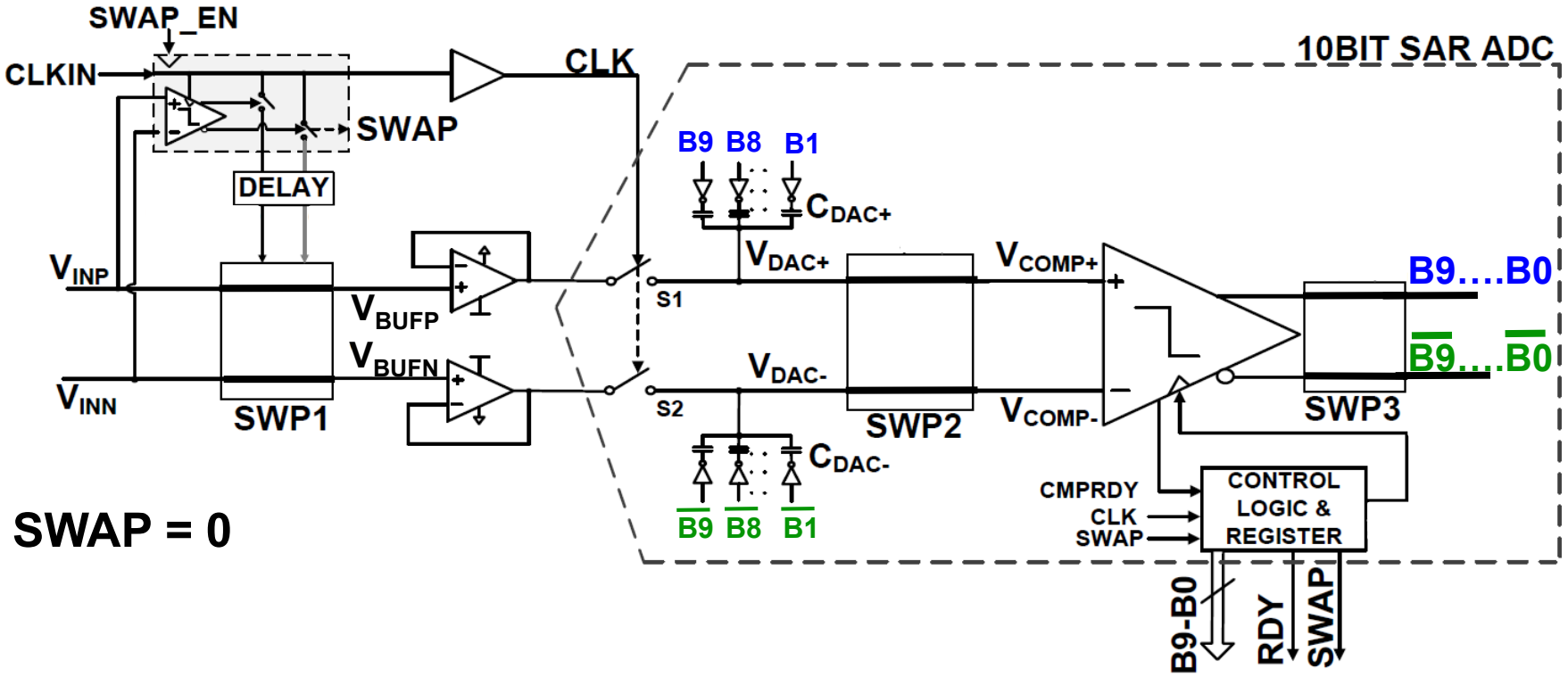

SWAP = 0

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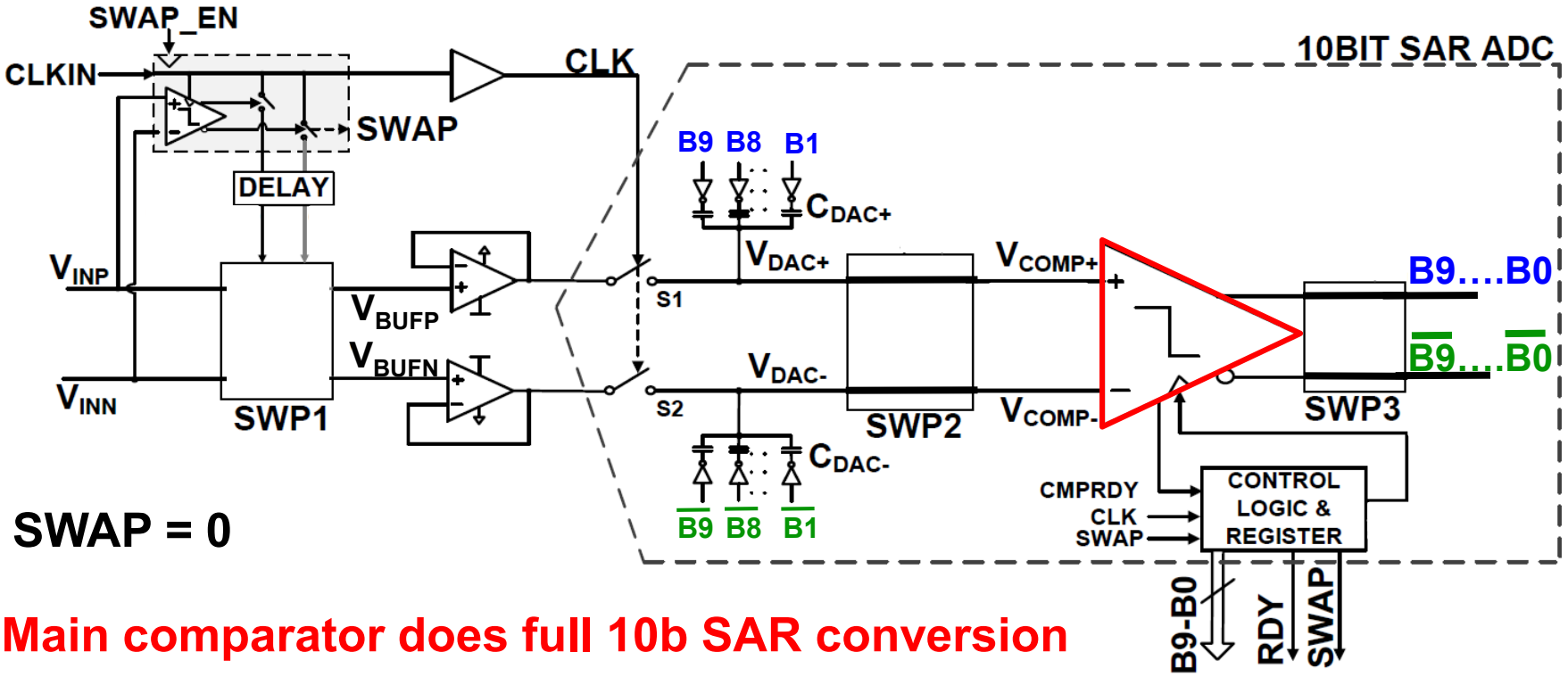
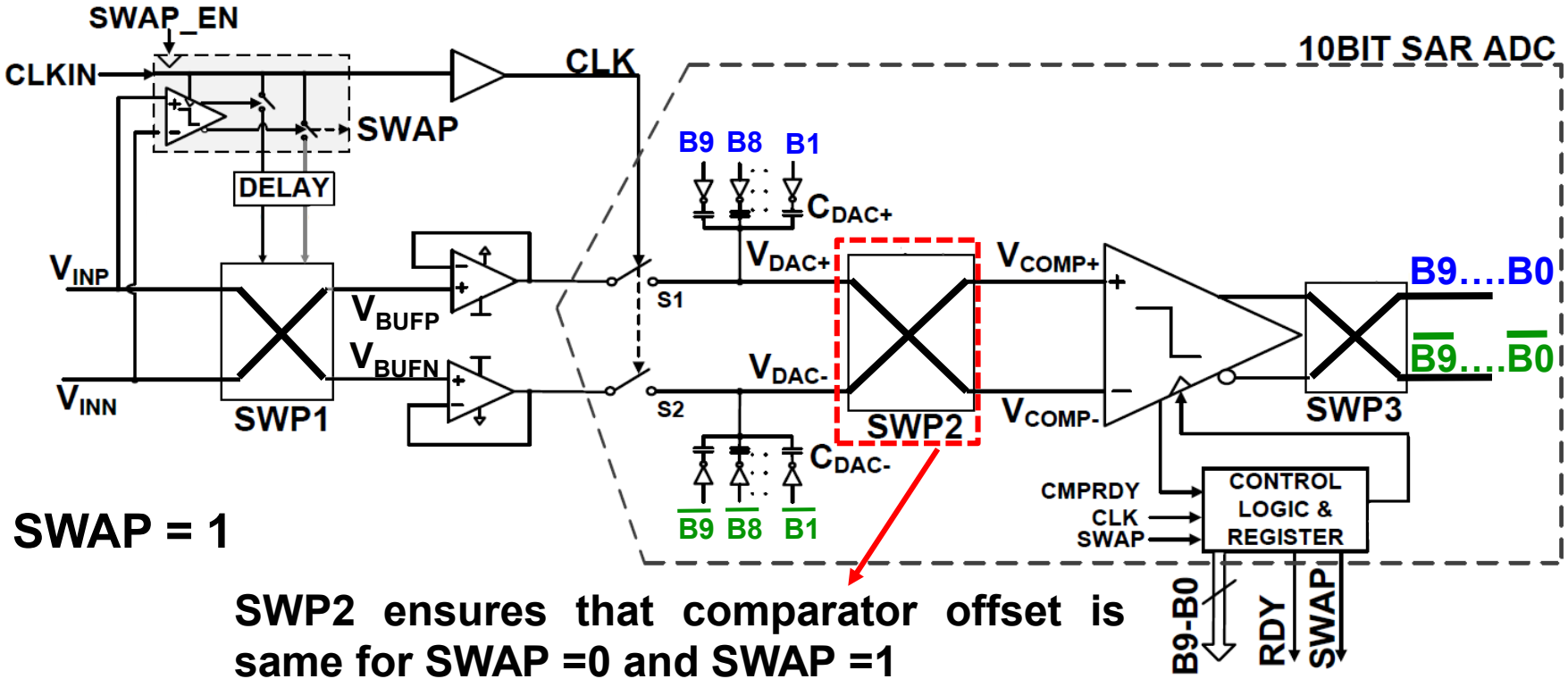


SWAP = 0

Main comparator does full 10b SAR conversion

Architecture - Buffers integrated with ADC



SWAP = 1

SWP2 ensures that comparator offset is same for SWAP =0 and SWAP =1

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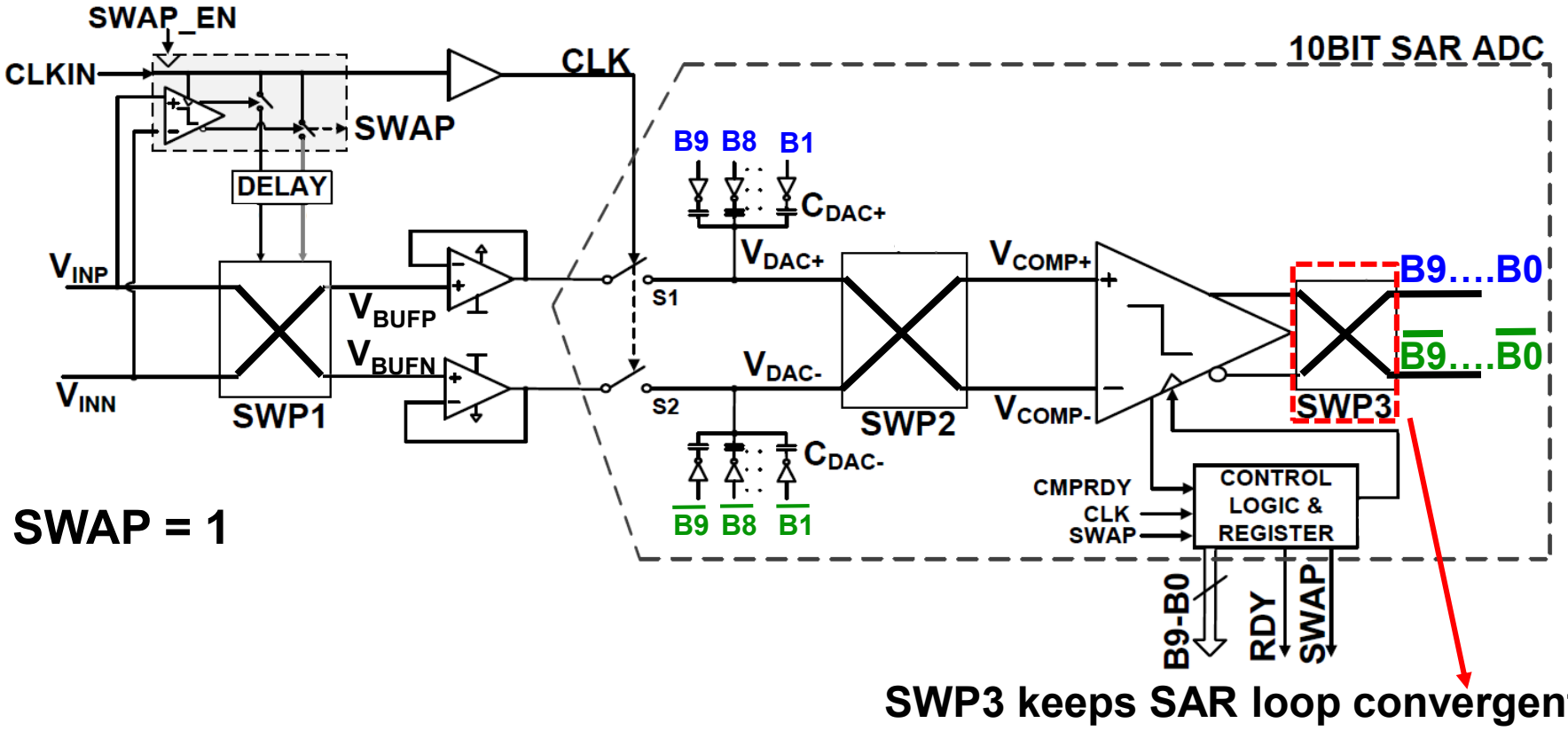

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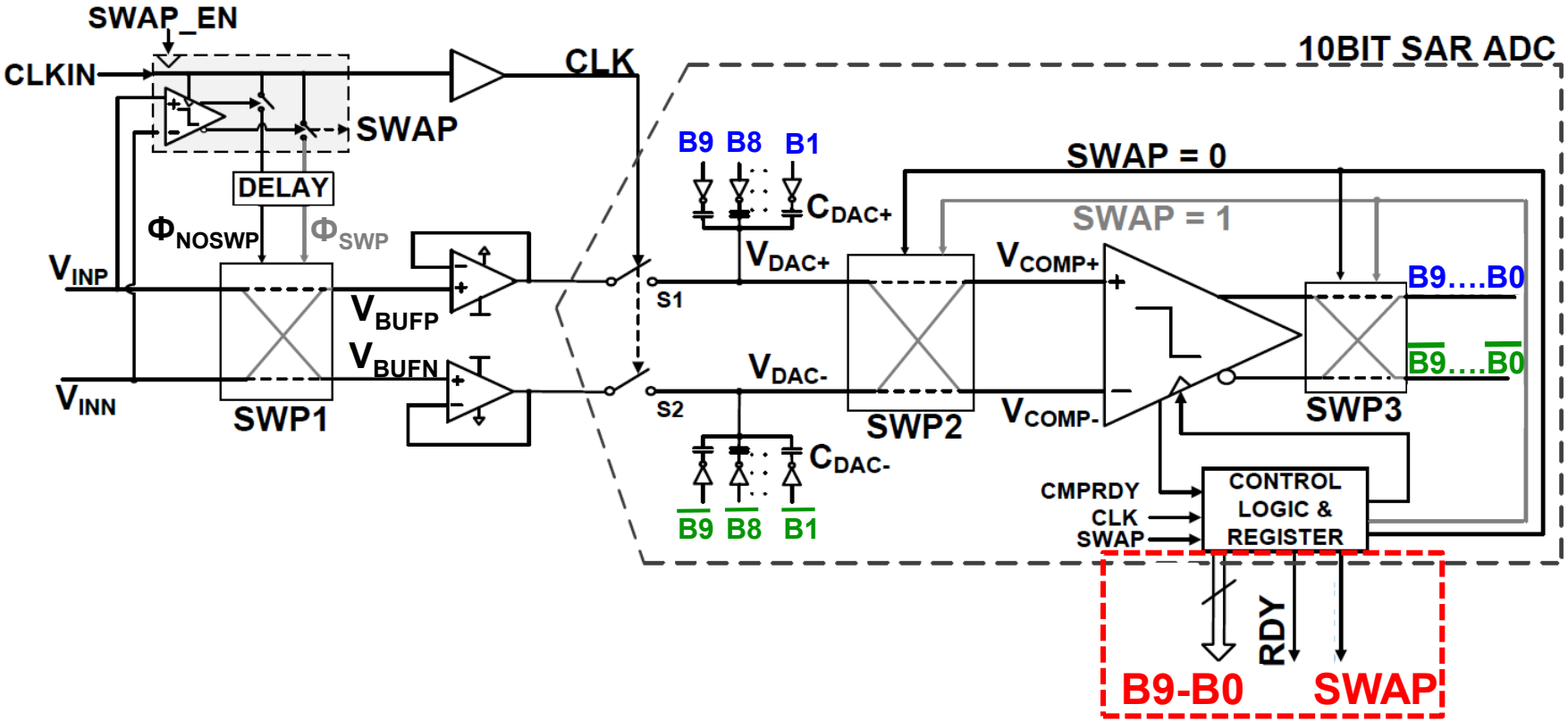
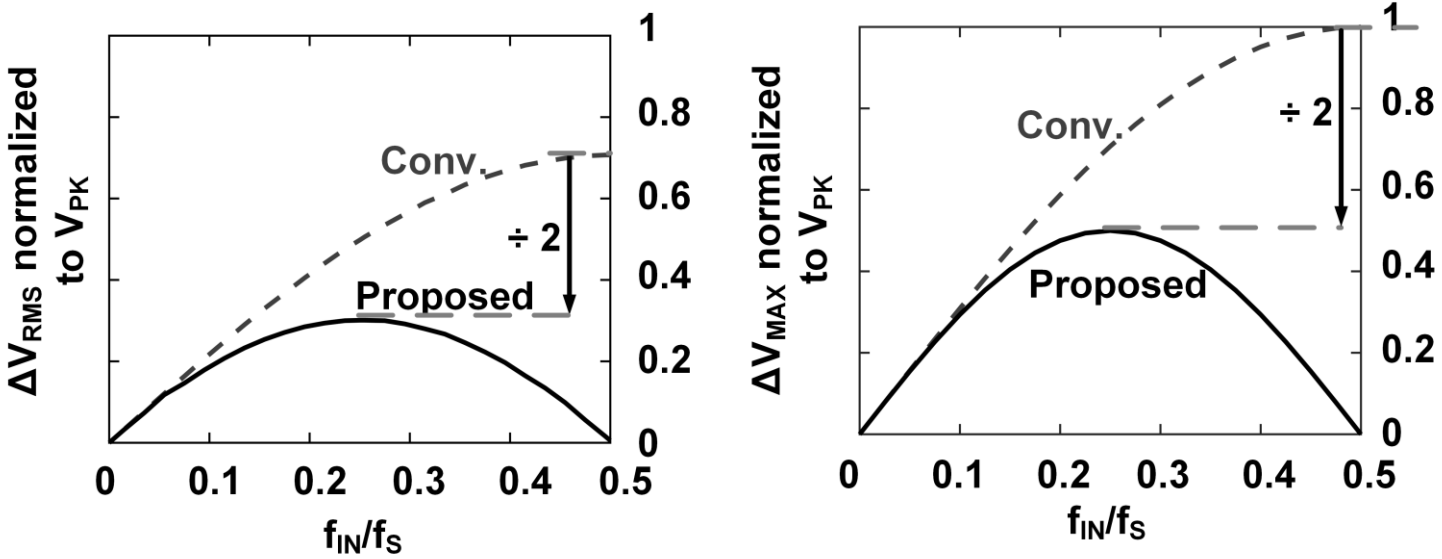


Change in voltage (V_{BUF} and V_{CDAC})

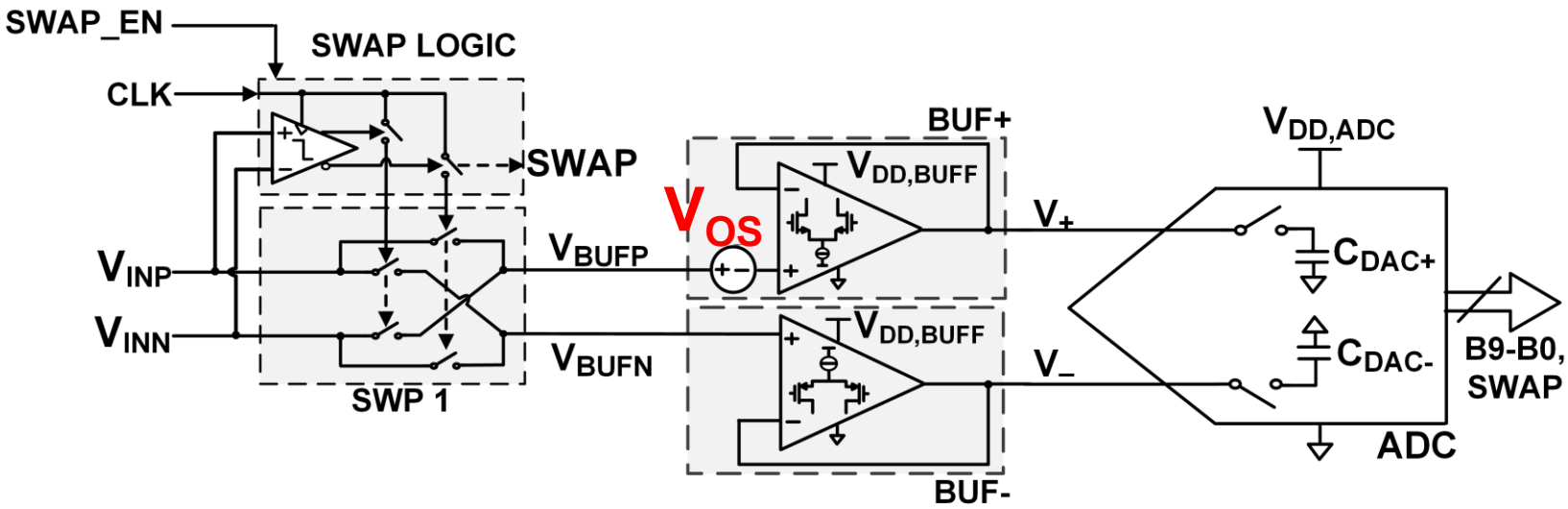


- MATLAB simulated RMS and maximum change in voltage at the buffer input
  - **Reduced by 2x compared to conventional sampling**
  - **$E_{IN} = C_{IN} \cdot \Delta V_{BUFP} \cdot V_{DD}$ is also reduced by 2x**

Overview

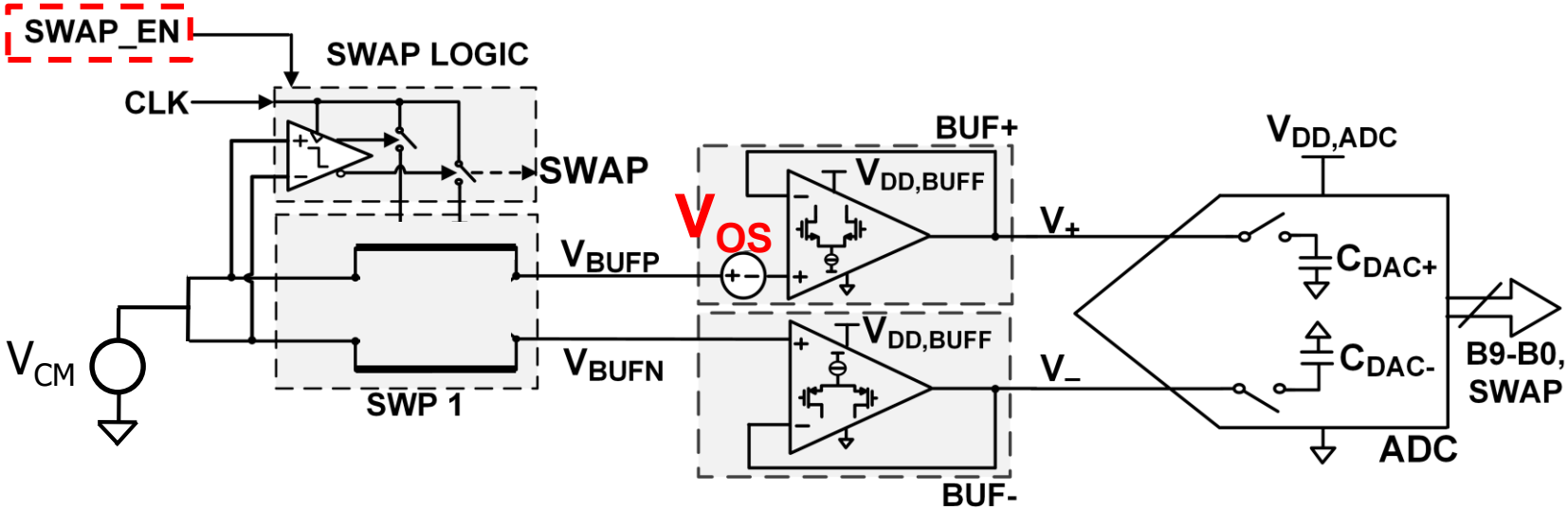
- Motivation
  - Input Buffer Requirement
- Reducing Input Drive Current
- **Low power single supply buffered SAR ADC (CICC 2019)**
  - Proposed Solution
  - Integration of Buffer with SAR ADC
  - **Offset Correction**
- Measurement Results
- Conclusion

Architecture - Offset Correction



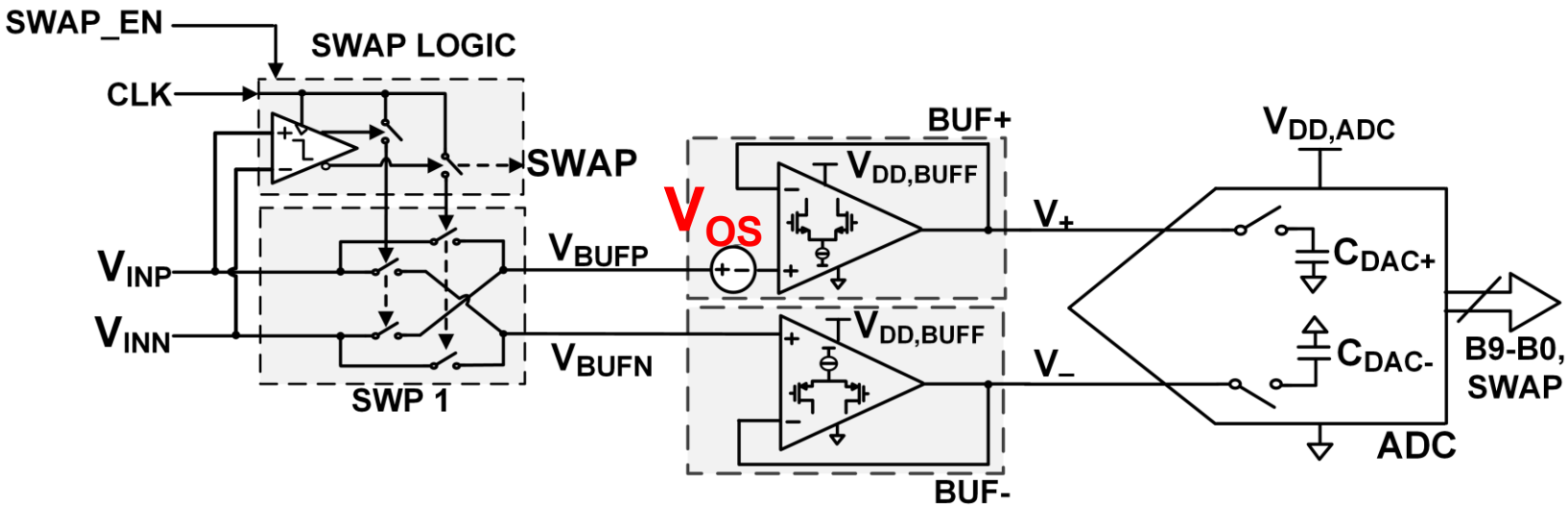
V_{OS} : offset mismatch between BUF+ and BUF-

Architecture - Offset Correction



$B_{OUT,OS}$: estimated by disabling SWAP and applying $V_{INP} - V_{INN} = 0$.

Architecture - Offset Correction



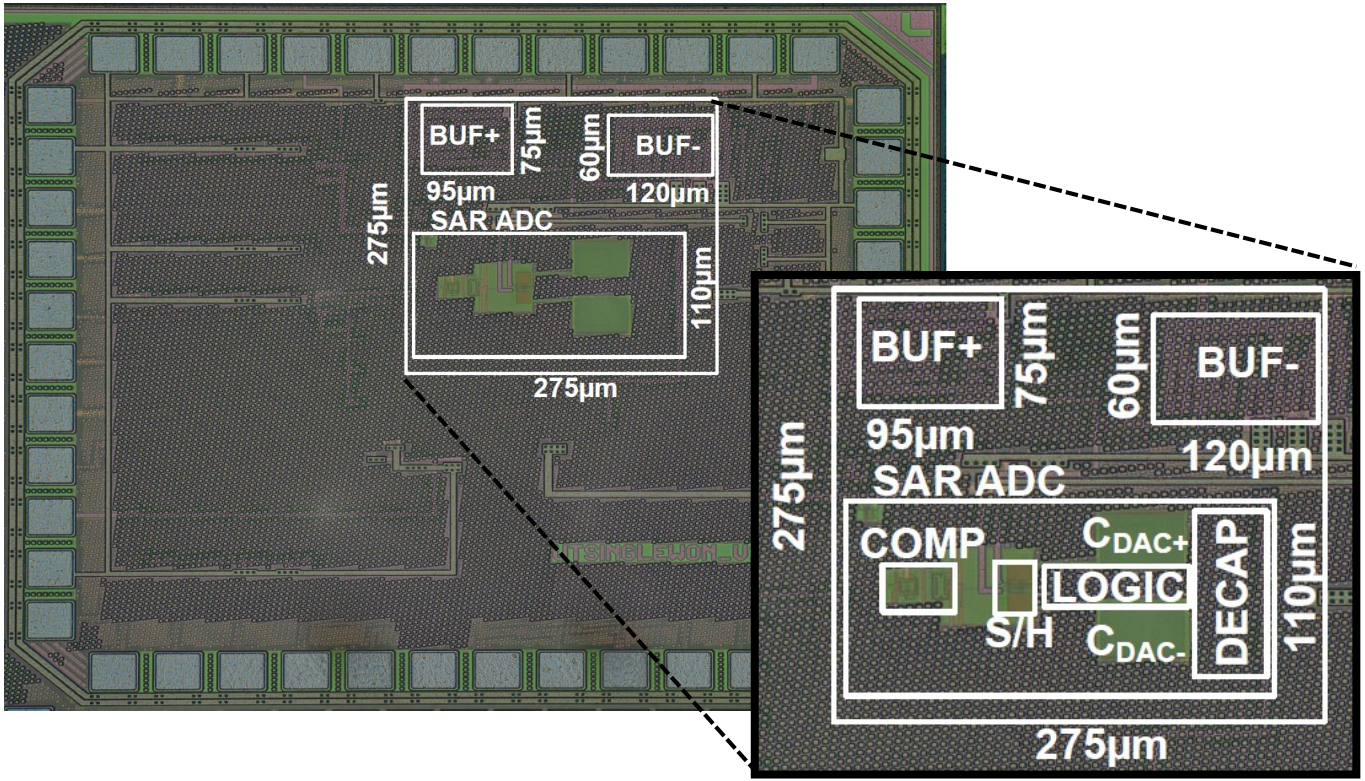
$$B_{OUT,SWAP} = \overline{B_{OUT} - B_{OUT,OS}}$$

$$B_{OUT,NOSWAP} = B_{OUT} - B_{OUT,OS}$$

Overview

- Motivation
  - Input Buffer Requirement
- Reducing Input Drive Current
- Low power single supply buffered SAR ADC
  - Proposed Solution
  - Integration of Buffer with SAR ADC
  - Offset Correction
- **Measurement Results**
- Conclusion

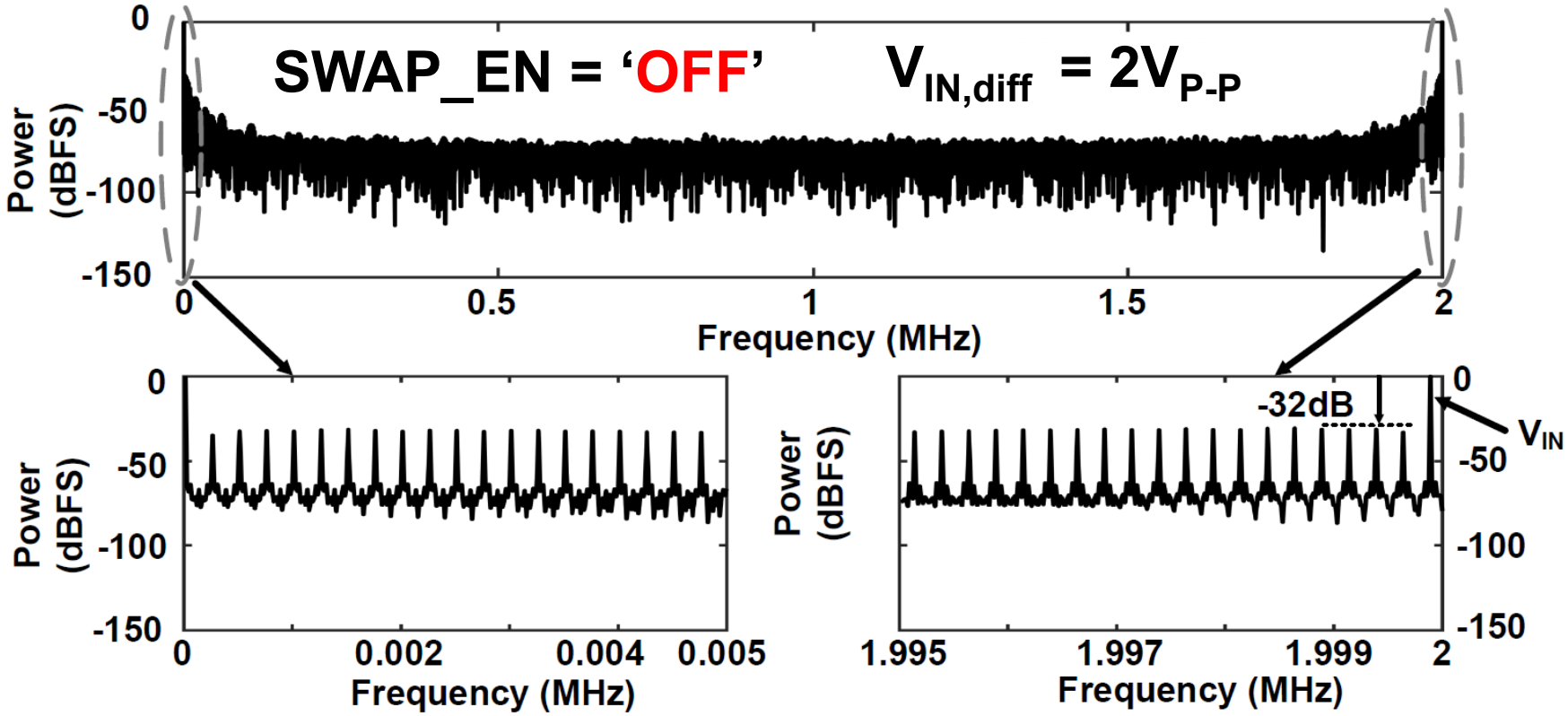
Die micrograph (65nm CMOS)



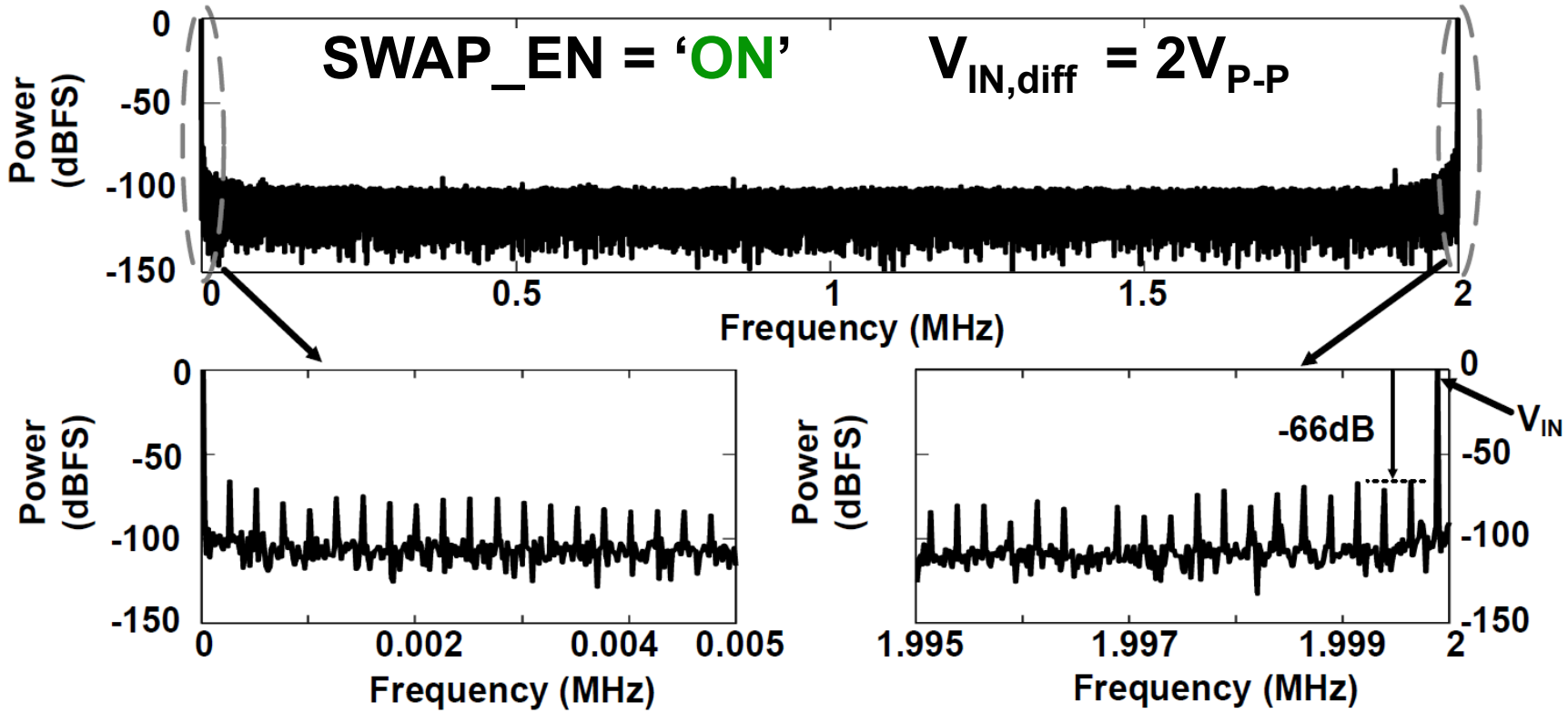
Area : 0.075mm²
(incl. decaps)

Power Consumption
ADC : 9µW
Buffers : 70µW each

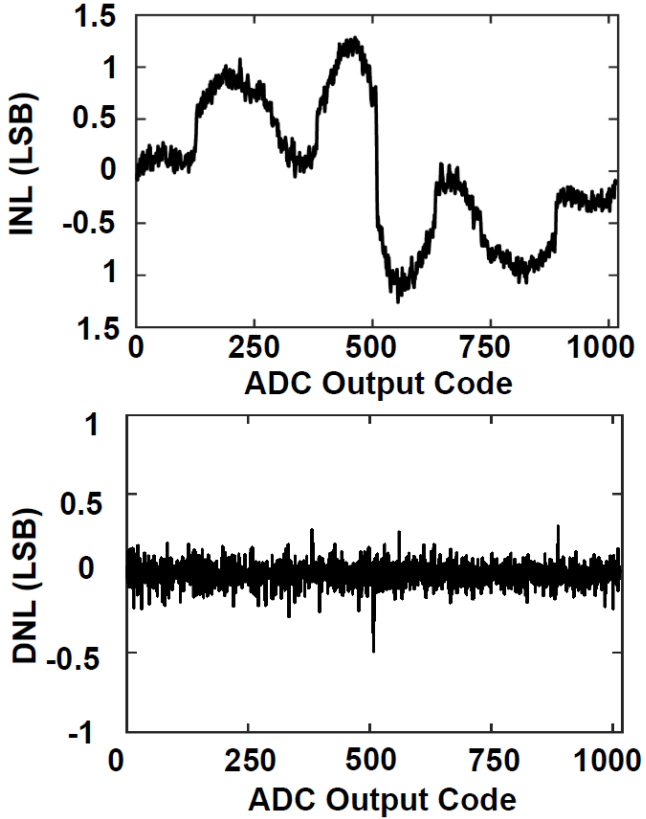
Measurement Results - FFT



Measurement Results - FFT

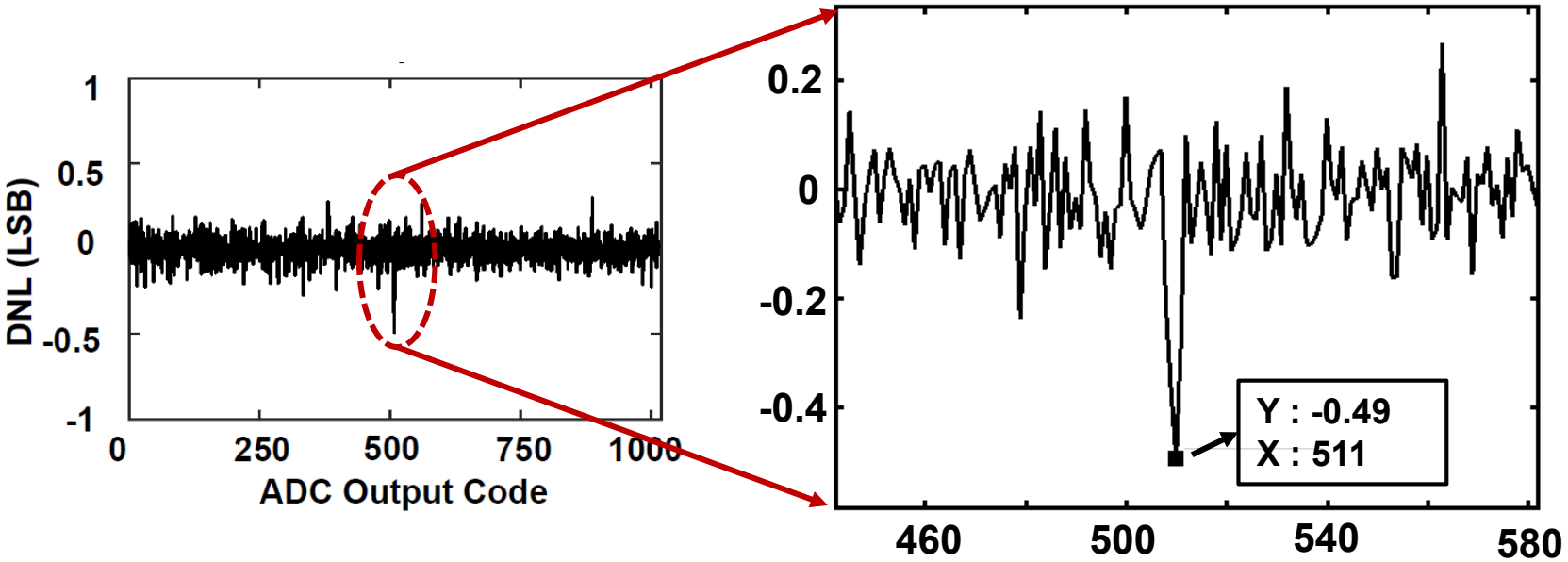


Measurement Results - INL/DNL



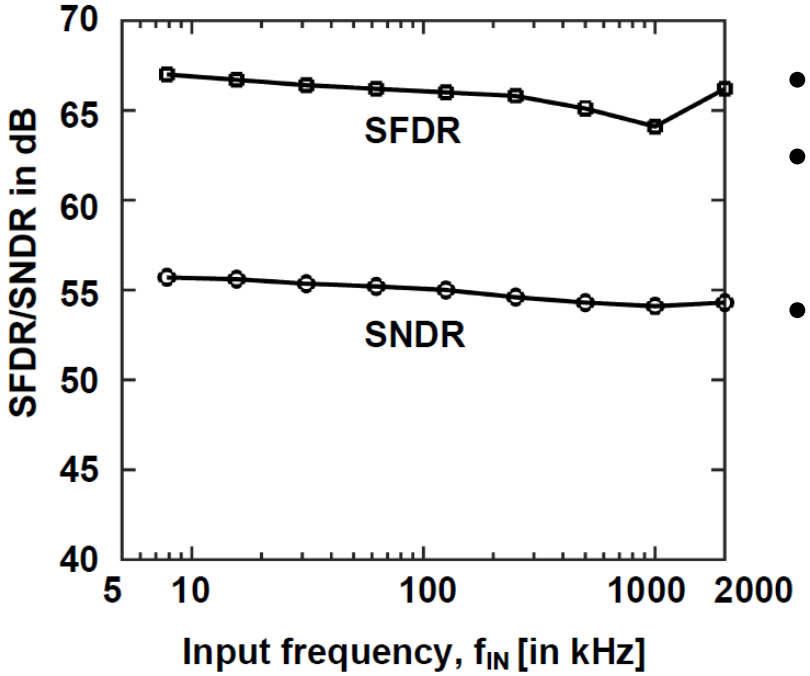
- f_S = 4MS/s
- INL = 1.2LSB
- DNL = 0.5LSB

Measurement Results - INL/DNL



- **Maximum jump is at mid-code due to non-segmented DAC array**

Measurement Results – SFDR/SNDR



- f_S = 4MS/s
- SFDR > 64dB over Nyquist range
- SNDR > 54dB over Nyquist range

Table of Comparison

Architecture		This Work	Krämer ISSCC 2015	Tseng JSSC 2016
Technology (nm)		65	40	28
Supply [V]	ADC	1.2	1.2	1.1
	Buffer		2.5	1.2
Diff. Input Signal (V_{PK-PK})		2	1.8	1.2
Maximum Sampling Rate (MS/s)		4	35	100
Power Consumption (ADC+Buffer) in mW		0.149	54.5	3.1
ENOB [bits]		8.7	12.1	7.2
FoM_w (fJ/conversion) = $(P_{ADC}+P_{Buffer})/2^{ENOB}.f_S$		87	355	200
Area (in mm^2)		0.075 (incl. decap)	0.24 (incl. decap)	0.024 (Core only)

Overview

- Motivation
  - Input Buffer Requirement
  - Prior Art
- Architecture
  - Proposed Solution
  - Integration of Buffer with SAR ADC
  - Offset Correction
- Measurement Results
- **Conclusion**

Conclusion

- **Buffers and ADC operate at single supply voltage (1.2V) while processing near rail-to-rail inputs.**
- **Swapping the inputs allow each of the input buffer to handle one-half the full-scale range.**
- **State-of-the-art Walden FoM (ADC+Buffer) of 87fJ/conv-step.**