Dynamic Life demands versatile Test Technology

Salland Test Technology Symposium 2019

SEPT. 26 - SEPT. 27

Welcome!

2nd Test Technology Symposium

SALLAND Engineering
Test Technology Center

provincie Overijssel

A warm welcome to our guests!

SALLAND Engineering
Test Technology Center

Salland Engineering at a glance

Test Application Solutions
- *Fast & Qualified new product introduction*

ATE Instrument Solutions
- *Industrializing your Test Solutions*

Supply Chain & Test Services
- *Delivering qualified Parts, Products & ATE Solutions*

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Supply Chain & Test Services

Delivering qualified Parts, Products & ATE Solutions

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Supply Chain & Production Test Services

Quick, Reliable & Independent Production Test including Test Engineering

ATE equipment

Teradyne UltraFLEX 24-slot
- RF UltraWAVE24

Teradyne UltraFLEX 12-slot
Teradyne FLEX-RF & µFLEX
Teradyne J750
- 1024 channel head

Exploring other platforms

Handling equipment

Wafer Probers (room to 150C)
- TEL P–12XLm for 6, 8 & 12“ wafers with hot chuck
- TSK-UF200 for 6” and 8“ wafers

Device Handlers (-60 to 150C)
- Exatron 903 Engineering handler, 3-temp.
- ESMO Talos Engineering handler, 3-temp.
- Chroma 3160C Production handler 3-temp.

Thermonics T-2500E

Services

Sample to mid volume testing
Final test and Wafer test
- 6, 8 and 12”

Characterization
Quality & Reliability analysis

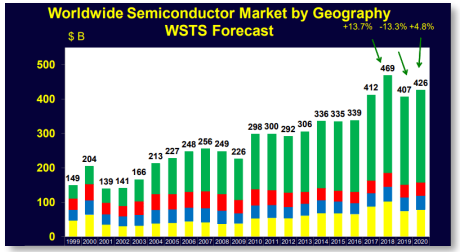
MASER ENGINEERING

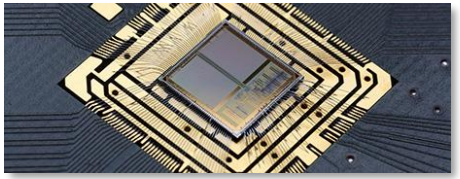
SALLAND Engineering
Test Technology Center

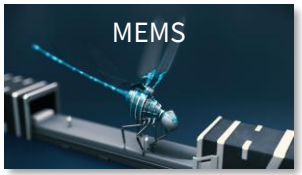
Today's Challenges

Many trends that push up development costs of ATE

- Semi market is growing but with 'ripples'
- Chip complexity increases
- ATE market is 'Stabilizing'
- Shorter life times
- New markets coming up
  - Specifications not well defined yet







Test Solution Development costs go up ➔ STTC idea born!

Intro/update to STTC

To boost your development by new Test Technology

- Last year we opened Salland Test Technology Center to *''Bridge to the future''*
  - Acquisition of APPLICOS a SALLAND Engineering Company to add 25+ years of Analog & PXI experience
- Development of ''fundamental test technology''
  - Including creation of IP-blocks ready to be used in products ELEVATE SEMICONDUCTOR
  - POC of complete test channels
- Exploring new test methods & technology to provide you
  - Faster Time-to-Market, Less risk and Lower costs to develop your products
  - *As we did over the last 27 years but at higher speed*
- Test industrializing and offering custom(er) solutions

Key is: Partnerships and collaboration

Close cooperation with MASER Engineering

Combined experience in Test, Qualification and FA Engineering ➔ in the past, present & future

SALLAND Engineering

- Test program & hardware development
- Electrical test of Qualification & RMA devices
- Broad range of testers available and accessible (including probers and handlers)

MASER Engineering

- Qualification, FA and RMA handling
- Full range of qualification equipment
- State of the art Physical Analysis lab for FA and RMA handling

- Seamless logistic flow between Salland and MASER, both located in the Netherlands (< 80km).
- Large customer base of IC development companies in OEM, IDM, Fabless, Design houses
- Know-how of qualification (Automotive (AEC-Q100) Industrial/Consumer (JEDEC)
- Both work independently with other test-houses and qualification labs

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Today: our role in the Test Technology Eco system…

Close cooperation with end customers and partners to deliver solutions that work

Technical Universities

Saxion University of Applied Sciences
University of Twente.
Windesheim
Tyndall National Institute
TU/e Eindhoven University of Technology
Fraunhofer

Consortia/Tech programs

PhotonDelta
EURAMET
High Tech NL
From RF to MMW and THz silicon SoC technologieS [RF2THZ SISOC]
TechWorks
semi
BCSEMI NL
DAISY

Manufacturing Partners

SallandElectronics
ELECT
NEWAYS
SAB Special Cables

APPLICOS
a SALLAND Engineering Company

Technology Partners

ELEVATE
Solidus Technologies, Inc.
multiLane
Photonic Integration Technology Centre
PICSL
MASER
CITC
Chip Integration Technology Centre

ATE & PXI Manufacturers

TERADYNE
ADVANTEST
Xcerra
National Instruments Alliance Partner
Chroma
MARVIN TEST SOLUTIONS
pickering
ASTRONICS

IDM, Fabless, Subcons

SALLAND Engineering
Test Technology Center

…makes us Partner of industry market leaders

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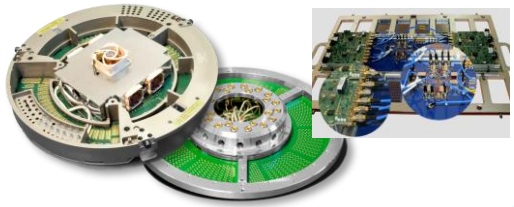
STTC projects

Building future-proof Test IP & Tooling to deliver **enabling Technology**

Salland Innovative milestones

Test Innovation over the last 25 years

- 1999: (First) protocol aware
- 2000: First Bluetooth production program
- 2003: 24 ➔ 256 DC channels for uC/CC
- 2004: 30 ➔ 192 DC channels for Cellphone Power management
- 2007: 16 ➔ 72 VI channels for Tablets
- 2013: 32Gbps SerDes on Catalyst/93k
- 2015: RF-modules to deliver 30GHz on Flex to Radar- Array
- Applicos: OEM MEMS test intrument



New and ongoing developments

Tooling and Test Technology that cover the real needs

- DPLUS – Tool for quick and advanced Data Analysis
- DPIN – High Density, low-cost Pin channel up to 500MHz
- LOW-CAPA – MEMS Testing without physical stimulus
  - Extreme low current & capacitance test circuitry
- SerDes – Test modules up to 100^{+}Gb (PAM4/x)
  - Including ATE-drivers, integration and application support
- Photonics – Exploring Test technologies together with our partners
- High Density DPS IP based on ElevATE component

DPLUS: Tool for quick and advanced Data Analysis

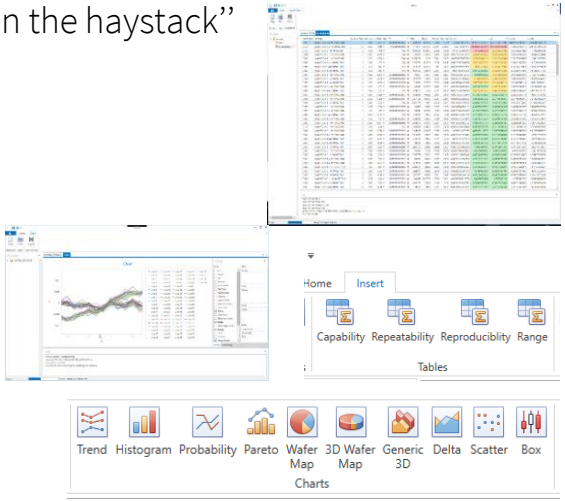
Easy to find ‘’the needle in the haystack’’

Tool for both Application and Instrument Engineering

- Quick analysis of large amounts of data
- Easy site/channel correlation & investigation ➔ find the ‘’needle in the haystack’’

Made by the inventors & creators of SEDANA

Not for plant optimization
or process control



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LOW-CAPA: Extreme Low Capacitance measurement IP

Addressing the MEMS, Sensor & IoT Market

Challenge: Test MEMS without physical stimulus

- Small capacitance and current
- Correlation between physical and electrical stimulus

Our approach

- Low capacitance and current IP
- Working with several stakeholders to prove PoC

Made our own MEMS device

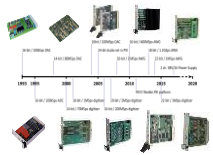
Instrument Target specification	
Capacitance Range	±5pF (0fF to 5000 fF diff.)
Settling time	3ms
Accuracy	~4fF
Resolution	18 bit (≈ 40 aF)
Carrier Frequency	30kHz to 2MHz
Carrier Waveform	Square
Carrier Amplitude	0.5V, 1V, 1.5V, 2V (rms)
Noise	±4fF
V DC Bias	±15V
No. of DC Bias Ch.	8
Number of Meas. Ch.	8
Phase Angle Meas.*	Not Supported
Max. cable length	1.0m

Salland will combine IP to offer new solutions

Most of the IP is already developed or is ongoing and needs to be combined

Partners: Sensata Technologies, SAXION Hogeschool, SRON Netherlands Institute for Space Research, University of Twente.

- Low capacitance
- Low current
- Processing power
- AWG/DIG
- RF/wireless

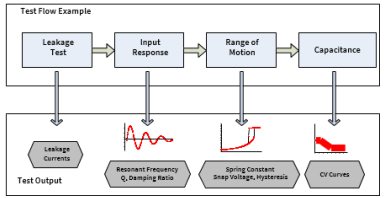


MEMS, Sensor, IoT Test Technology

- Modules
- PXIe card
- ATEx/SLT

Solidus Technologies, Inc. — MEMS Test Equipment & Semiconductor Engineering

MEMS Test Technology



Target markets

- MEMS
- IoT
- Sensors

DPIN - Challenges in IO channel development

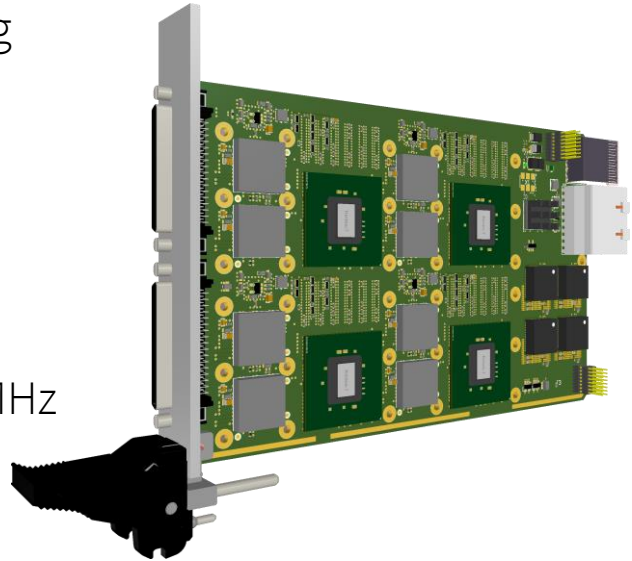
Development of high density & low cost IO - IP

Challenge: Get as many IO channels on a card as possible

- Space, Power, Cooling, Connections/interfacing

Our approach

- Evaluation kits
- POC 8 channels
  - FPGA based timing generator
- Test vehicle: PXI card format with 64ch @200+MHz



Photonics – New test technology

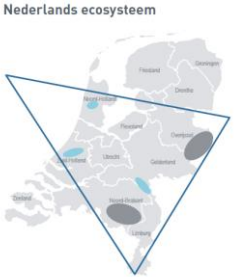
Challenge: Test optical-electrical components at standard Semi supply chain

- High speed IO sources
- Light sources
- Signal delivery

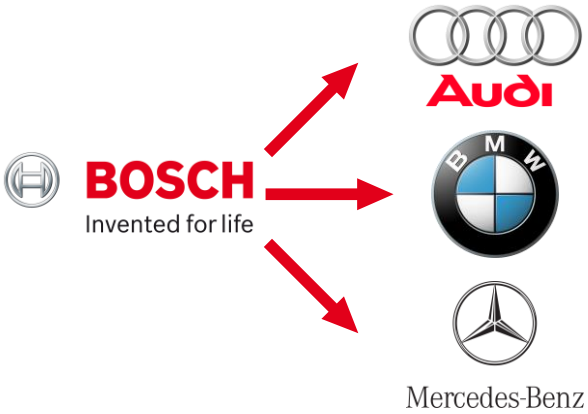
Our approach

- How to deploy existing technology to deliver a complete solution
- RAAK: how to interface
- PITC: data management and deliver test solution

We participate in PhotonDelta Integrated Photonics Ecosystem



STTC ambitions – What BOSCH does for automotive…



Thank you!