SALLAND Engineering

Test Technology Symposium 2019
Program Thursday, September 26

09:00-09:30 Registration and coffee/tea

09:30-10:00 Opening & Welcome Test Technology Symposium

Paul van Ulsen - Salland Engineering

Paul is responsible for all aspects of corporate governance for Salland Engineering worldwide. Paul joined Salland in 1993 as a Test Application engineer. He became Manager of the Test Application business unit and soon demonstrated his sales skills as Managing Director for Salland Europe. Prior to Salland, Paul worked for Rood Testhouse International as a mixed-signal application engineer. He is a graduate of Windesheim Technical University in electronics and computer engineering.

IC DESIGN & TEST CHALLENGES

10:00-10:30 Low Energy Design techniques for Data Converters

Harijot Singh Bindra - University of Twente

Analog to Digital Converters (ADCs) are crucial to capture data in almost any Internet of Everything (IoE) device as sensed physical signals have to be converted into digital data, before some processing and data transmission can take place. Today, ADCs are designed for low supply energy consumption, usually expressed in energy-per-conversion step which for state-of-the art architecture is (stagnated) ~ 1fJ/conversion-step. However, the energy consumed from the always ON sensor interface circuitry e.g. the input driver is usually not taken into account and seldom addressed. This input drive energy (usually larger than the ADC supply energy) presents a major challenge in minimizing the energy consumption of e.g. autonomous and event-driven IoE applications. In this talk a few a few silicon-proven techniques are presented that can significantly reduce the overall power consumption of the buffer/driver + ADC.

Harijot Singh Bindra received his Master's in Technology degree in VLSI design from Indian Institute of Technology (IIT), Delhi in 2010. He worked as a Scientist in the Indian Space Research Organization (ISRO) from 2008-2010 and as Senior Design Engineer at Cadence Design Systems, India from 2012-2014. He is currently working towards a PhD degree at the Integrated Circuit Design group, University of Twente, The Netherlands. His research interest is in low energy circuit design techniques.

10:30-11:00 A flexible evaluation platform for a novel X-ray detector

Charles Klaasen - Bruco

An important part of the development process of any Integrated Circuit (IC) is of course real-life measurements on the bench. Creating complex chips, requires increasingly complex ways to test these chips on the bench but also in production. Working with start-ups, next to the technical challenges, the NRE costs and flexibility of the test environment might even be more important. Bruco Integrated Circuits has successfully developed a very flexible and programmable evaluation set-up that allows our customer G-ray Medical to validate their LateniumTM X-Ray detector. This detector is a state of the art 72k pixel-array X-ray image sensor. Our evaluation kit handles different variants of a family of these image sensors. For our customer it is a product that they sell to showcase their X-ray image sensors and their associated, patented wafer bonding process. For Bruco it is a flexible platform that we want to re-use to serve other customers. See https://www.bruco-ic.com/solutions/x-ray-detector-read-out-system.

After graduating for his Master's degree in Electrical Engineering back in 1998 at the University of Twente Charles started his professional career as a digital IC engineer designing embedded DSPs for Philips Semiconductors in Eindhoven. For a period of 10 years, he developed a number of chips as member of design teams of Philips, Ericsson, in Enschede and Emmen working on base stations and Bluetooth, Vitratron in Arnhem, working on pacemakers, before joining design house Bruco Integrated Circuits in 2005. Bruco Integrated Circuits is a SME that provide IC design services and develops turn-key chips for large and small international customers. In 2008 Charles took on a new role as Account Manager within the Sales and Marketing team of Bruco. Since then he is the interface between customers, the Bruco team and partners as Salland Engineering.

11:00-11:15 SHORT BREAK

11:15-11:45 Challenges in High voltage IC design for ATE applications

Jef Thoné - MinDCet

The drive for reduced carbon emissions and high electrical efficiency is pushing the supply voltage levels and the adoption of Silicon Carbide (SiC) and Gallium Nitride (GaN) transistors in power conversion solutions. These wide-bandgap devices have beneficial properties when hard-switched, that translate into challenging requirements for the ATE equipment that needs to measure them. In an ideal world the requirements can be summarized as an idealized spice simulation : zero on-resistance, infinite off-resistance, zero inductance, zero capacitance, no physical footprint, infinite voltage capability, infinite transient immunity, zero dissipation, perfect thermal conduction, infinite lifetime… and always ready for the next generation of high-voltage DUTs. As high-voltage designers, we translate the requirements into real-world specifications, by making the best trade-offs possible. This is based on available technology, but mainly based on hands-on experience, in-house developed tools, parasitic extraction tools, electronic and field simulators. High-voltage IC design is a complex craft, combining high-end analog design, new state-of-the-art topologies and years of experience into challenging solutions that enable the next-generation high-voltage ATE equipment. This presentation treats the primary challenges met in high-voltage IC design in the context of the world of ATE.

Jef Thoné received the Master of Engineering degree in Electronics at the Karel de Grote Hogeschool in Antwerp, Belgium in 2002. From 2002 to 2006 he was employed as ASIC designer and project manager at Melexis Belgium, where he cooperated in the analog design and production of several automotive ASICs. In 2006 he joined the Sensor Systems Research Group of ESAT-MICAS of Prof. Puers, Katholieke Universiteit Leuven, Belgium. His PhD entitled "Telemetry for Capsule Endoscopy" was concluded in 2011 and focused on high data rate biocompatible telemetry systems and wireless power transmission. In 2011 he co-founded MinDCet NV, a Power Conversion design house, together with Mike Wens.

11:45-12:15 Image Sensor testing, ByS or BaS

Peter Crabbe - AMS Sensors

CMOS imaging sensors from ams feature global and rolling shutter capability, low noise, high dynamic range and high frame rates. Offering an integrated design, the sensors include a high-speed on-chip ADC and digital interfaces. ams offers its imaging sensors as complete turnkey solutions, and the whole process from specification and design, through prototyping and product qualification, to volume production, is implemented by ams. Manufacturing and Test of Image sensors is an “art”. The Manufacturing and Test strategy needs to be carefully chosen and has a strong link on the volumes to be delivered.
This paper will compare 2 approaches in respect to test of Image sensors

Peter Crabbe is Director of Operations at ams Sensors Belgium. He holds a Master Degree in Microelectronics and an Executive MBA from the University of Antwerp. Previously he worked at Salland Engineering in the Netherlands as COO and before that, he held various positions at Alcatel Mietec, AMI Semiconductor and On Semiconductor in Belgium and the Philippines.

12:15-12:45 Structure of modern SDR - Lime's field programmable RF devices

Danny Webster - Lime Microsystems

Software defined radio (SDR) gives the freedom to develop flexible, reconfigurable radio systems that can embrace the wide range of radio standards that have been rapidly evolving since the 1990s, including 4G, 5G and WiFi MIMO systems for telecommunications and data links, as well as transmitters and receivers for commodity type products such as DAB, DBT, DBS, GNSS etc. etc. This talk will describe the structure of modern SDR together with the architectures of Lime's field programmable RF devices, which can cover from longwave to milimeterwave.

Dr. Danny Webster has over 25 years of experience in the field of RF Communications including software defined radio, mobile radio and military telemetry. Danny graduated from Swansea University in 1988 and was awarded a PhD from University College London in 1995. From 1995 he has worked as a Research Fellow at University College London and was a consultant to companies such as Nokia, Roke Manor Research and Agilent (Keysight) in Santa Rosa. From 2001 he was with Hipertech and joined Lime Micro in 2005 as Principle Design Engineer (RF) working on Field programmable RF ICs and software defined radio. Danny is a senior member of the IEEE.

12:45-13:30 LUNCH

SEMICONDUCTOR ECO-SYSTEM IN NL

13:30-14:00 Dutch Semiconductor ECO-system

Barry Peet - BCSemi NL

Barry Peet will give insight into the Dutch Semiconductor ecosystem. An overview of what’s going on in the Netherlands, from Chip-design to manufacturing, equipment and last but not least testing. An overview of the companies and institutes and what activities BCSEMI NL coordinates and executes to stimulate the growth of this ecosystem. An ecosystem that gives us the name ’Small Country, Semicon Giant!’ abroad.

Mr. Barry Peet has a Master degree on Electronic Engineering. He has 12 years of experience in running his own mobile ICT company, were he was responsible - as founder and COO - for sales, project management and managing the software development team. Mr. Peet is now managing director of Business Cluster Semiconductors Netherlands (BCS), the Dutch semicon cluster that supports a total of more then 60 companies and knowledge institutes and strives to achieve competitive advantages for companies active in the development, production and application of Advanced ICs, MEMS, Sensors and Wireless Systems by collaboration.

14:00-14:30 Aspects of semiconductor component assembly

Roland Tacken - Neways

The link between Neways and the semicon industry can be seen from two perspectives. As an electronic manufacturing provider, Neways supplies PCB and hybrid assemblies to the semiconductor equipment manufacturers. At the same time, Neways processes the products of the semicon industry: packaged silicon SMD components, bare dies and MEMS. In this presentation, aspects of the electronic assembly proces will be discussed with a focus on chip handling and ceramic based substrates.

Ir. Roland Tacken has a track record in the high tech industry and holds over 15 international patents and a dozen of publications in the field of materials and materials processing technology. After graduating in Chemical Engineering at the Eindhoven University of Technology, he started his career in process engineering within the optical media industry (Toolex/Singulus) and managed the R&D team in CD, DVD and Blu-ray process development. Next, he set up a R&D group working on thin film technology for electronic and solar applications at TNO Science & Industry. After serving as senior project manager for flexible solar lines at VDL-ETG he moved to the electronics manufacturing industry. Now, Mr. Tacken is managing the engineering department within Neways Micro Electronics B.V.

SALLAND Engineering

Test Technology Symposium 2019
Program Thursday, September 26

TEST TECHNOLOGY & TOOLING

14:30-15:00 Just another fabless startup making a chip using standard processes at TSMC and ASE...?

Paul Elford - Graphcore

Not quite. AI chips for inference that go into server farms in amongst huge GPUs, CPUs and network processors have engineering challenges that established companies might have already solved, but the solutions are not necessarily well known across the industry. This leads to a lot of discovery-led engineering problem solving. I will describe some of these, focussing especially on those that arise in the area of test.

Paul Elford is currently in charge of Production Test Outsourcing in Graphcore, working on the next generation of AI processors. He has over 25 year experience in Semiconductor Product and Test Engineering roles. Starting as a Product Engineer in GEC Plessey he has worked for a variety of companies from raw start-ups to establish multi-nationals; including Directing the Product and Test Dept of the Semtech LoRa IoT Product line. Paul has a BEng(Hons) in Electrical and Electronic Engineering from the University of Plymouth.

15:00-15:15 SHORT BREAK

15:15-15:45 Introduction to our New Test Data Analysis Tool

Johannes van Putten - Salland Engineering

Within the ATE industry, the amount of collected data is growing rapidly. It is important to process your test data fast with the least possible effort. Computers grow better over years, but software existing in the market is not able to take advantage of this power. Salland built a brand new data analysis tool, made for engineers, by engineers. Built from scratch, it uses the latest technologies. It is fast, intuitive, feature rich and reads all common test data formats and produces charts with a single click. The new tool automates common workflows that test engineers often have to go through. Salland will continue to extent the tool with new features, such as single click reports and smart algorithms that detect problems in your test data

Johannes is Senior Software Engineer and Lead Engineer of the project. He completed a Bachelor's degree in Electronics with specialization in Embedded Systems. With over 30 years of work experience, he started in Electronic Design and over time shifted to Software Engineering. His fields of expertise are Software Architecture and Functional Programming with extra interest in Machine Learning.

15:45-16:15 Mechanical Design of Contactor footprints: Limitation of the Electrical vs Mechanical trade off

Peter MacMichael - PTSL

As the design and manufacture of Test Interface solutions or ATE Probe Cards and Load boards, as they are more commonly known, become more complex, the need for close collaboration between the mechanical designer and the electrical designer become increasingly important. This is to ensure a seamless and timely process flow through the whole design process from initial RFQ stage through to the mechanical contactor design and PCB design through to the end manufacture of a deliverable HW solution. In this presentation, we take a look at the various different types and elements of ATE probe card contactor's for wafer level test and the various socket contactor types used for package level test and the different implications that the mechanical design can have on the electrical design of the PCB board or vice versa. We also take a look at why FEA analysis for mechanical stresses and thermal heat analysis can also have an important impact in the overall design. The intention is to give both mechanical designers and PCB designers, who often reside in different departments or even different companies a better understanding of what is required to create a successful ATE probe card or final test load board solution.

Peter is Business Development Manager at PTSL. He has over 20 years' experience in ATE hardware, having held Mechanical Design, PCB Design, Applications Engineering, and Sales positions within the industry before taking on his commercial role leading PTSL Customer Operations in Europe.

16:15-16:45 Cloud-based Collaborative Characterisation and Guardband Generation

John O'Donnell - YieldHUB

Traditionally desktop tools dominate the analysis of new silicon test data even through to the generation of the characterisation reports themselves. Spreadsheet tools such as Excel have been used extensively. Such tools are subject to human error and because of this, careful preparation is required taking days even several weeks in some cases to arrive at a clean and accurate report which can be shared with design and marketing. The cloud brings a new opportunity to revolutionize such report generation through closer collaboration and faster generation of the final clean report to within hours of the data being ready. This presentation will describe how yieldHUB has worked with several multinationals to streamline characterisation through a collaborative cloud-based platform that incorporates Knowledge Sharing, on-line Collaboration, Data Cleansing and the integration of Target Cp/Cpk as well as Virtual Retest. Guardband generation is also considered when the main factors contributing to variance are available. Also discussed is how test datalogs can be made compatible with this system and the speed of report generation when thousands of tests are involved.

John started in test development and then worked in product engineering. He has presented at numerous conferences and has several patents in test technology. A father of four, he enjoys following rugby and Gaelic football. He and his family like to holiday in France every year and also enjoy travelling to different parts of the Wild Atlantic Way during the summer in Ireland. John's work brings him all over the world and he particularly enjoys meeting test and product engineers at the front line of new product introduction and when an exciting product they are working on is ramping fast.

16:45-17:15 PIC (Photonics Integrated Circuits): adding automated testing to automated assembly

Stefan Schlörholz - ficonTEC

18:00-18:45 GROUP PHOTO & TOUR AT SALLAND ENGINEERING FACILITY

19:00 SOCIAL NETWORK EVENT - drinks and dinner

Test Technology Symposium 2019
Program Friday, September 27

08:30-09:00 Registration and Coffee/Tea

NEW PRODUCTS & TRENDS

09:00-09:30 Low capacitance test solution

Armando Bonilla Fernandez - Salland Engineering

The complexity and number of devices that need to be tested increases with the development of new technologies. The use of MEMS devices is an example of the areas that is continuously growing. Nowadays, one of their biggest applications is in the sensing field, where MEMS are used to develop pressure sensors, accelerometers, gyroscopes, inertial combos, etc. For such sensors, a capacitive read-out is preferred in many cases due to its advantages, which include low temperature coefficients, low power dissipation, low noise and low-cost fabrication. One of the main challenges of MEMS devices' fabrication is the fact that high-volume testing normally requires custom-made test set-ups, due to its multidomain composition. In this session, we will discuss a proof-of-concept to check the feasibility of integrating a low capacitance measurement into an Automatic Testing Equipment (ATE). For this proof, special attention has been paid to the distance between both the paired Device Under Test & Measurement system and the multichannel instrument implementation. Based on this proof-of-concept, our aim is to optimize the testing procedure for a wide range of MEMS devices.

Armando has a Bachelor degree in Mechatronics from the UANL in Mexico with 3 years of experience in industrial automation. He received the MSc degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2016, with specialization in Robotics and Mechatronics. In 2017 he joined Salland Engineering (Europe) B.V. where he focuses on Design Verification of electronic instrumentation and hardware design.

09:30-10:00 Testing for the Next Generation

Patrick Sullivan - ElevATE

The demands of tomorrow will push the need for disparate sensor technology, greater processing power, higher communication rates and greater storage capacity. This explosion of technology will create greater demands on tester capabilities and flexibility which in turn impact their ability to control the cost of Test. Elevate Semiconductor believes success depends on properly architected and designed ICs that interface with the DUT (device under test). This talk will briefly outline how Elevate is evolving to facilitate the next generation of test.

Patrick Sullivan holds a Bachelors degree in Electrical Engineering from The University of Wisconsin – Madison. He has designed analog chips for A.T.E applications for 25 years while working at Brooktree, Edge Semiconductor, Semtech, Planet ATE and Intersil. Mr. Sullivan was a cofounder of Edge Semiconductor and Planet ATE.

10:00 - 10:15 SE-DPIN: Challenges in IO channel development

Harry Ramaker - Salland Engineering

In the ATE industry, the complexity of devices increases significantly while on the other hand the cost of test must decrease. This can be achieved by testing more devices in parallel and/or increase test speed. For this the number of resources that are available in ATE must increase as well (more channels, higher speed and lower cost/channel). The principle of digital cards in ATE has been the same over many years. The only difference is the speed, the number of tester channels and some additional features such as scan patterns. With DPIN the number of channels on a small surface increases (2.5 cm2 /Channel) by means of standard components that are available in the market. The FPGA is a flexible solution to implement a timing/formatter. DPIN hardware accepts Vector, Formats and Timing information (after compilation) that are used by the standard ATE to test latest technology chips.

Harry is Senior Firmware and Lead Engineer of the <DPIN> project. He started working for Salland Engineering in 1994 in the instruments development group and has over 20 years of experience in developing Firmware for XILINX FPGA's. He completed a Bachelor's degree in Electronics in 1983. Before he joined Salland, Harry worked 10 years for Rood Testhouse. His fields of expertise were writing digital test programs on different ATE tester platforms (J941/T7341..) for incoming inspection mostly for military/automotive/space and industrial applications.

10:15-10:45 **Expediting custom ASIC design & supply via proven partnerships**

David Wright - Adesto

Adesto Technologies (formerly S3 Semiconductors), delivers efficient silicon design to ASIC delivery by utilising our proven supplier partnerships and integrating our extensive portfolio of in-house silicon proven mixed-signal and RF IP. With custom ASICs, OEMs can enable their product vision with the development of a single chip that delivers the performance they need for their application. The chip is unique to them and offers security of their IP while saving board space and cost by up to 80%. Adesto deliver on this by using expertise from our experienced designers in the USA and Europe and our Fab, Assembly & Test partners in Europe and Asia. Customers desire seamless design and manufacturing cycles, and, as a unique provider of combined design, IP and ASIC supply, we enable this by giving the customer direct access to the teams who manage design, test, qualification and supply of the ASIC.
In this session, we will chart Adesto's growth, and how it has delivered on a number of ASICs by partnering with Salland to achieve development of production test solution and subsequent management of production test and delivery from their site, on schedule and within budget. We will focus on two customer engagements which showcase our expertise and trusted supplier relationships and give our customers confidence in our ability to enable them delivery of their product.

David is currently Senior Product Test Engineer in the AID Division of Adesto Technologies. He has worked in the semiconductor industry since 1983, having graduated from the Dublin Institute of Technology in the field of Electronic Engineering and Communications. He worked as Product Test Engineer for Fujitsu Microelectronics in Dublin's DRAM and EPROM manufacturing plant supporting the production from wafer-saw through Assembly and Test all the way to warehousing. He experienced the technology progress from a 16KB DIP to a 16MB TSOP, over 14 years, before moving to Xilinx Ireland, where he supported the FPGA production test of the Spartan and Virtex architectures for 12 years, before supervising the transfer of those product lines to Xilinx Singapore. At Xilinx he held the roles of Senior Product Test Engineer and Product Engineering Manager. He was recruited by Adesto in 2016 to implement Test and Qualification supply chain of the ASIC supply business, and has successfully brought a number of ASICs to production, in both Mixed-Signal and RF technologies.

10:45-11:00 SHORT BREAK

PRODUCTION SUPPLY CHAIN

11:00-11:30 **Qualification Test definition based on application and product mission**

Kees Revenberg - MASER Engineering

The applications of electronic components and systems is continuously expanding. They are present in safety critical applications in humans (medical), cars (breaking/airbag) and industry (aerospace/powerplants). Also the amount of less critical applications is increasing. Product qualification procedures and methods need to be adapted to address this wide range of application environments without overstressing the electronic devices or systems. This presentation will show the approach MASER Engineering is taking to secure an optimal qualification program.

Kees Revenberg is co-founder and managing director of MASER Engineering. His primary focus fields are the corporate strategy, sales & marketing and finance. He graduated as BSc in electronics in 1982 at the University for Applied Technology in Zwolle, The Netherlands. He started his career as a chip test program developer with an independent test house in the Netherlands, followed by the start of their Quality & Reliability test services and managed that department for five years until the company stopped its activities in 1992. After starting MASER Engineering in 1993 he co-developed the company to a significant player in Europe for independent Test & Analysis services of micro-electronics with a central laboratory in Enschede, the Netherlands and sales offices in United Kingdom, Germany, Belgium and Israel.

11:30-12:15 **Ag-sintering and its impact on power electronics**

Marco Koelink - Boschman

Ag-sintering is a new but proven and accepted new (die-) bonding technology that provides cost advantages, performance and reliability. It is currently mainly being applied in automotive power electronics for electric vehicles (EVs). But the expectation is that the electrification of cars - with this disruptive technology - will in turn drive enabling solutions and reliability throughout the entire electronic supply chain. This presentation will explain some of the technical background of the technology and provide an overview of some of the ongoing trends in the market of automotive power that Ag-sintering is driving.

Marco Koelink holds a PhD/MSc in Applied Physics from the University of Twente and an MBA from Tilburg University. He has diverse experience with a.o. Philips and NXP in semiconductors, display technology, solid-state lighting, medical, and industrial equipment. His previous roles include Development Manager for NXP RF Power; Director of Materials Analysis for Philips Research; and Market Intelligence Manager for Philips Lighting. As a Business Development Manager, Marco is currently responsible for marketing and sales activities at Boschman Advanced Packaging Technology.

12:15-12:45 **Test processes in PIC production chain: challenges and solutions**

Dr. Weiming Yao - TU Eindhoven

Increasing maturity and accessibility of photonic integration technologies allows such to penetrate into a wide range of applications. Photonic integrated circuits (PIC) are used in a variety of products for tele and data communications, sensing including automotive, aerospace, agriculture and healthcare. This results in an increased demand in terms of throughput and cost efficiency of manufacturing chain of such PIC based products. National and international initiatives such as the JePPIX pilot-line, ACTPHAST prototyping and the Photon Delta integrated photonic ecosystem stimulate further growth of the PIC industry and enable next generation developments to cope with the demand. Highly automated tools and processes, including electronic-photonic test are required at all stages of the product creation chain, from a design to assembled module. A new class of test tools and methods is needed to enable optimization of the fabrication and assembly processes as well as functional verification at system level. Such will lead to increased throughput, yield at product level and cost efficiency. Challenges with respect to electronic-photonic testing in the PIC manufacturing ecosystem will be discussed.

Weiming Yao received the B.Sc. in Electrical Engineering from the Technical University Berlin, in 2010, and the M.Sc. in Photonic Networks Engineering from Aston University, UK, and Scuola Superiore Sant'Anna, Italy, in 2012. Since 2012, he is working in the Photonic Integration Group (PhI) of Eindhoven University of Technology (TU/e), the Netherlands and obtained a Ph.D. degree in 2017 for work on integrated high-capacity optical transceivers. Since 2017, he is with the Photonic Integration Technology Centre (PITC) where he is leading a national open innovation development line project for fabrication of photonic ICs (OpenPICs) and has responsibilities in the EU InPulse Pilotline. He has (co-) authored more than 30 publications in international journals and conferences in the field of photonic integrated circuits.

12:45-13:30 LUNCH

SALLAND Engineering

Test Technology Symposium 2019
Program Friday, September 27

AUTOMATED TEST

13:30-14:00 Testing AI devices: Challenges and Trends

Martin Dresler - Advantest

Artificial intelligence (AI) is utilized across a wide variety of applications and control systems, from complex self-driving cars to the less complex monitoring of a production process. Advances in processing power, networking transfer speeds and the ability to collect and save huge amounts of often unstructured data known as big data enables deep neural learning. This presentation will address some technology trends in the different areas like cloud, automotive and edge processing and how this effects ATE instrumentation, SW and test methodology.

Martin Dresler, MSEE and MBA, works at Advantest Europe and has more than 20 years of ATE experience in the areas of mixed-signal, high-speed digital, high-speed memory and RF in different positions. As Business Manager, he is now leading the worldwide performance digital team activities including AI and high-performance compute.

14:00-14:45 Laser Diode used in 3D sensing, technologies, test requirements/concerns and solutions

Jeff Lee - Chroma ATE

3D sensing is widely used for biological ID, AR, environmental modeling for portable devices, Gamming, Autonomous or even military applications. Among different 3D sensing technologies, Laser Diode is constantly selected as illumination light source. This talk helps audience understand the various 3D sensing technologies, provide pros&cons, and the role that Laser Diode plays in various approaches. Then the test requirements and concerns will be elaborated together with commonly seen solutions.

Jeff Lee has over 27 years of experience in Test & Measurement, PV, LED, LD & Turn Key Solutions for Power Electronics. He is Co-chair of SEMI Taiwan PV Standard Committee (2008-2012) and currently VP of Sales / Marketing, ISS BU, Chroma ATE Inc in which he is leading Chroma 3D sensing test solution and co-work with world-leading Face ID companies.

14:45-15:15 ATE Test Solution for Automotive Bus Systems

Mike Bergler - Cohu

The number of electronic components in vehicles has increased rapidly and continuously during recent years. On the one hand many new sensors and actuators and therefore new electronic control units have been developed to make passengers feel safer. On the other hand, entertainment and navigation systems have made their way into cars to make travel more comfortable. The path towards autonomous driving will enhance this trend. To meet the design challenges due to the different requirements (capacitance, real-time operation and cost), several bus systems have been developed or improved over the years. Automated Test Equipment (ATE) offer flexible test solutions and dedicated instrumentation at high levels of test parallelism and cost efficiency to cover the various test specifications. It simplifies testing of automotive bus devices at a decreased program complexity providing full test coverage and reliability. The presentation compares test methods and solutions by means of some automotive bus examples.

With over 20 years of experience in semiconductor industry, Mike Bergler is currently Director in the Cohu business development group. Mike's primary focus is growing the business for the Cohu ATE (Automated Test Equipment) products in the Power and Analog market space. His last role in LTX-Credence/Xcerra before joining the business development group in 2015 was ASL product specialist in the marketing group and prior to the merger of LTX and Credence in 2008 manager of the EU applications team. Before joining Credence in 1999 Mike was employed with the Automotive division of Siemens serving over 5 years test planning and quality management positions. Mike graduated in Electrical Engineering from Georg-Simon-Ohm University in Nuremberg. He is married with two children and lives in Stein, Germany.

15:15-15:45 5G Test strategy challenges

Deron Gerow - Teradyne

Emerging 5G devices for smartphones and infrastructure equipment present a more complex list of test requirements compared to current generation wireless devices resulting in test strategy challenges for the manufacturing and test organization. This presentation will provide an overview of these test challenges, considerations and test insertion strategies for 5G mmWave manufacturing test. In addition, it will provide an overview of Teradyne's recently introduced MX44 instrument to address characterization and production device testing for probe, package, over-the-air and module applications.

Deron has over 18 years of experience in ATE RF hardware development at Teradyne, and in his current role is the manager of the AC, RF, and mmWave instrument hardware development organization. He started his Teradyne career as a PCB and FPGA designer, and at various times has been a project lead, hardware engineering manager, RF systems engineering manager, and manager of Advanced Instrumentation. He has directly contributed to the development of 4 generations of RF products across 5 platforms as well as the newly introduced 5G mmWave test instrument, the MX44. Prior to Teradyne, Deron was a Staff Engineer at the MIT Lincoln Laboratory, developing RF receiver hardware for airborne platforms.

16:00 SOCIAL EVENT - drinks and snacks

END OF THE SYMPOSIUM