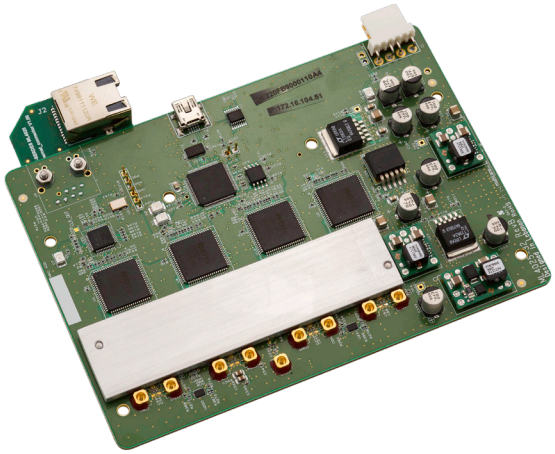
SALLAND Engineering
Test Technology Center

HSI-DSO-32

4 channel Digital Sampling Oscilloscope usable for Channel testing



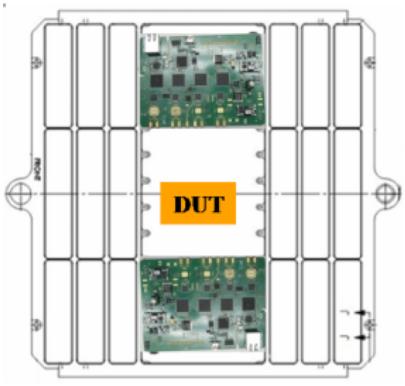
Key features

- Low cost quadruple 32 GHz Digital Sampling Scope optimized for high speed data analysis
- High Fidelity Signal Capture
- Low intrinsic Jitter
- ATE friendly interface and user friendly GUI
- Ultra compact form-factor along with low power consumption
- External (SMPM) and Internal reference clock input
- Single ended and differential electrical inputs for each of the four units
- Color graded persistence in Eye and Pattern capture modes
- In order sampling comparable with ATE platforms, when operated in bypass mode
- Ability to analyze and load data that you capture into the Simulator
- Capability to save statistical measurement and data files for multiple DSOs
- Full eye measurement can be attained in tens of milliseconds

Salland Engineering's HSI-DSO-32 is a state of the art quadruple 32GHz Digital Sampling Oscilloscope, ATE friendly, which automatically performs accurate eye-diagram analysis to characterize the quality of transmitters and receivers, implementing a statistical under-sampling technique with comprehensive software libraries used for eye measurements, jitter analysis and processing of NRZ data, designed for characterization as well as manufacturing.

Targeted Applications

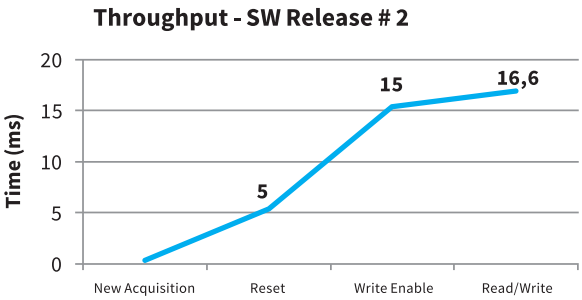
- Can be mounted on Automatic Test Equipment load boards, verified to fit into various ATE platforms such as the Teradyne (Catalyst, J750, UltraFlex), or the V93k
- High-Speed SerDes Testing & Characterization
- Design/Verification of Telecom and Datacom Components and Systems



SALLAND Engineering
Test Technology Center

- Electro-optical Transceiver Testing
- Handheld 10-25 G test equipment for field Installation and maintenance
- Multi-port system testing or Line Cards
- In-Suite testing of high port count systems
- Telecoms Equipment Test for Installation and Maintenance
- Fiber Channel, Ethernet, PON, Parallel Optics
- High port count burn-in test

High Test Throughput



Measurements

- Total Jitter & Jitter decomposition: DJ, RJ
- Mask Margin, Alternate Mask; Margin rules available
- The mask margin (positive or negative) can be extracted for a defined number of points that fail, thus allowing for DUT quality assessment, control and binning
- The number of failed points for a region can be returned as well as the actual points that failed
- Eye opening, eye height and width, eye amplitude, top, base, max, min, peak to peak

- Rise/ Fall Time, Single Edge measurement in pattern capture Electro-optical Transceiver Testing
- Statistic histograms and histogram measurements
- Crossing percentage
- Pre-emphasis positive and negative (amplitude and width)
- Advanced Pattern Measurements
- Eye measurements on specific properties of the pattern
- Zooming, markers, X & Y histograms, overlays and multiple measurements, statistics

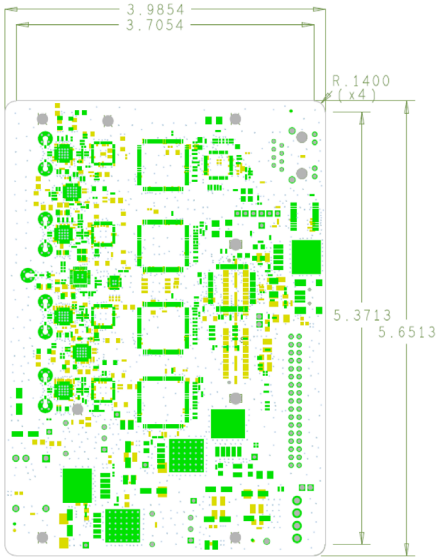
Deliverables

Hardware:
- HSI-DSO-32 module

Software:
- Windows GUI and API access by 3rd party software
- Function libraries for ATE platforms:
  - For Windows, incl. DLL and C++ header files containing the Interface Classes
  - For Linux: incl. library documented socket interfaces and Interface Classes

Manuals:
- User Manual (Incl. installation)
- API function library description & usage calls

Board Dimensions



SALLAND Engineering
Test Technology Center

Specification

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Bandwidth					32	**GHz**
Input Amplitude		S.E.			600/1200	**mVpp**
Input Rise / Fall Time (20% to 80%)	tRT, tFT			14		**pS**
Vertical Resolution				12		**Bits**
Clock Input range (normal mode)			10kHz		750	**MHz**
Clock Input range (bypass mode)			10kHz		125	**MHz**
Clock Input Amplitude		S.E.	200		1000	**mV**
Input Impedance	Z			50		**Ω**
Intrinsic Jitter (excluding DDJ)		Note1			200fS	**rms**
Amplitude Error (rms)		Note2		4		**mV**
Data Format supported				NRZ		
PRBS Pattern Capture		Note3			PRBS13	
Spurious-Free Dynamic Range (sine wave)	SFDR			8		**Bits**
Memory Depth				256k		**Samples**
Power requirements				12V DC @ 1.6A		
Calibration				Quarterly calibration recommended		

Notes

1. Intrinsic jitter is the additional jitter uncertainty of the DSO as the statistical sum of sampler, and the timing generator and DSO interconnect.
2. Related to calibration time @ 600mV input over operating temperature range.
3. For all measurements that require pattern lock. For all other measurements the DSO supports up to PRBS31.

SALLAND Engineering
Test Technology Center

Salland Engineering is an international leading Test Technology & Engineering company specialized in solutions & services that enable semiconductor manufacturers to achieve Lower cost of test, Higher quality and reliability, Improved test floor efficiencies, Faster time to market and Streamlined supply chain. Salland Engineering is in business since 1992, headquartered in Zwolle – The Netherlands, and operates worldwide.

- Supply Chain services from **prototyping**, **manufacturing** up to **repair service** for **advanced measurement** solutions **on site** in The Netherlands
- **ISO 9001:2015** certified