(some) IC Design Innovation

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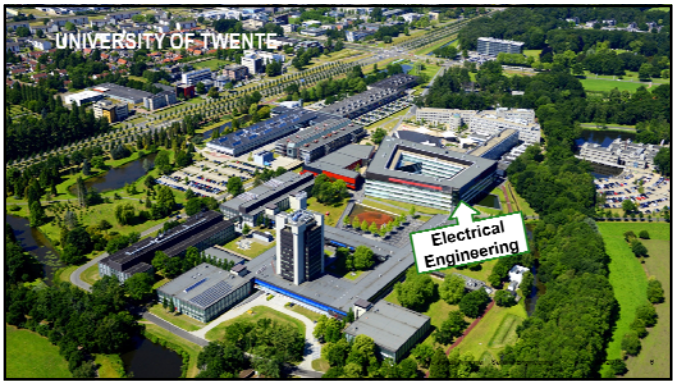
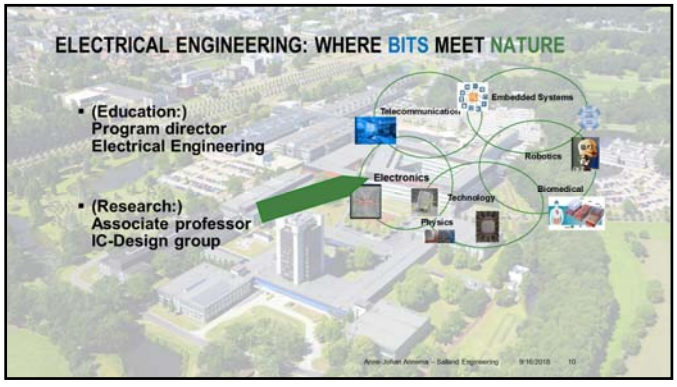
CONTENTS

- University of Twente
- Electrical Engineering
- IC-Design group

- Some examples of circuit innovation
  - Intro
  - How to improve SAR ADC performance
  - Class-E RF power amplifiers
  - Wrap up





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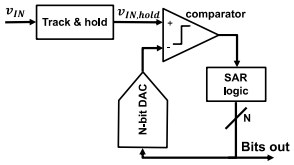
SUCCESSIVE APPROXIMATION REGISTER ADC: OPERATION PRINCIPLE

- Track & hold
- DAC
- comparator
- binary search



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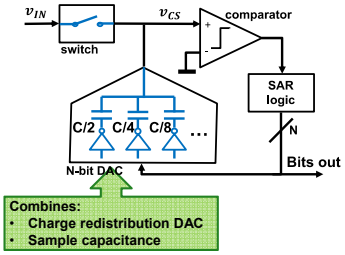

Combines:
- **Charge redistribution DAC**
- **Sample capacitance**

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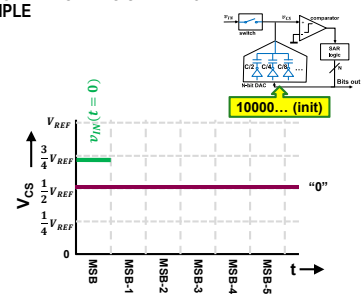

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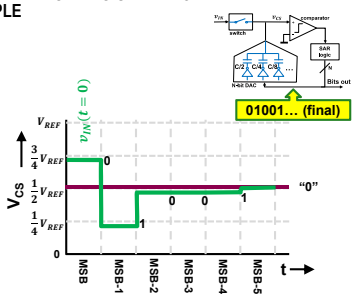
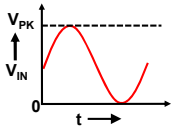
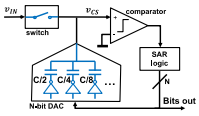


SUCCESSIVE APPROXIMATION REGISTER ADC: METRICS





Dynamic Range (DR) = $\frac{\text{max signal power}}{\text{noise power}}$

- Noise power = thermal noise
- ~~Noise power = quantization noise (#bits)~~

FUNDAMENTAL LIMIT(ATION)S -1

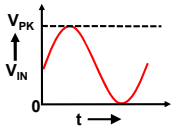
From statistical physics:
- $E_{thermal} = \frac{1}{2}kT$

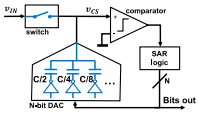
Energy in a capacitor:
- $E_{stored} = \frac{1}{2}Cv^2$

Thermal noise on a capacitor ($E_{thermal} = E_{stored}$):
- $\overline{v_n} = \sqrt{\frac{kT}{C}}$

Lower noise ↔ larger capacitance

SUCCESSIVE APPROXIMATION REGISTER ADC: METRICS

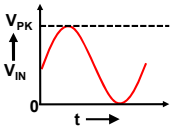


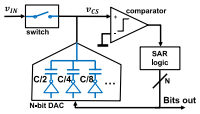


Dynamic Range

- DR = $\frac{\text{max signal power}}{\text{noise power}} = \frac{{}^{1}/_{2}\cdot V_{PK}^2}{{}^{kT}/_{C}} = \frac{C\cdot V_{PK}^2}{8kT}$ (thermal noise limited)
- More DR: higher V_{PK}=V_{DD}
- More DR: higher valued C
- More DR: lower T

SUCCESSIVE APPROXIMATION REGISTER ADC: METRICS





Dynamic Range

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Modern CMOS… Power !!

Coolers

FUNDAMENTAL LIMIT(ATION)S -2

Energy stored in a capacitor:
- $E_{stored} = \frac{1}{2} Cv^2$

From electrical relativity:

Energy required to charge (resistively):
- $E_{dissipate} = \frac{1}{2} Cv^2$

Repetively (e.g. sine in, switching)
- $P_{charge} = f_{signal} \cdot C \cdot v^2$

SUCCESSIVE APPROXIMATION REGISTER ADC: HOW TO IMPROVE THE FOM

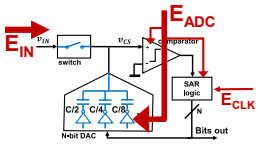
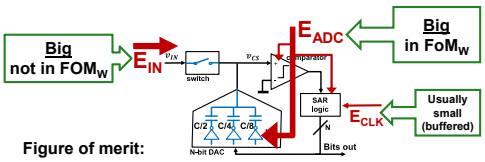


Figure of merit:

- $FoM_W = \frac{E_{ADC}}{2^{ENOB}}$
- use different f_{signal} for E_{ADC} and ENOB
- energy scavenge on v_{in}
- energy scavenge on CLK

- **Really make it better…**

SUCCESSIVE APPROXIMATION REGISTER ADC: HOW TO IMPROVE THEM



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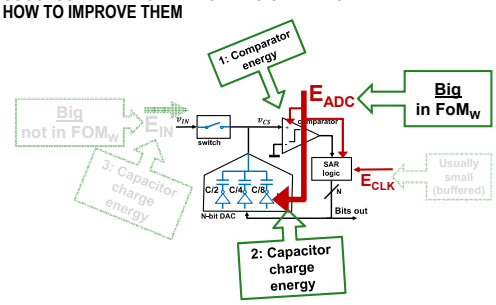
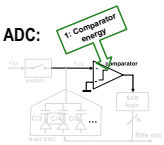


SUCCESSIVE APPROXIMATION REGISTER ADC: HOW TO IMPROVE THEM - 1

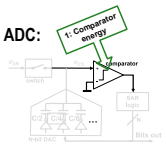


Comparator:

- Time discrete operation
- "low noise"
- Low <u>energy</u> (time discrete!)

→ Charge (energy) biased Clocked operation

SUCCESSIVE APPROXIMATION REGISTER ADC: HOW TO IMPROVE THEM - 1



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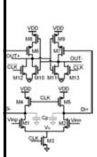
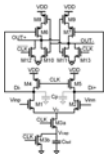
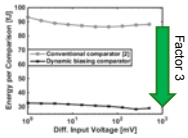






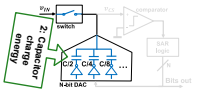
ventional
linkel, not crowbar)

Hosticka - 1980

Our version design

Benchmarking with SOTA

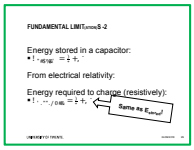
SUCCESSIVE APPROXIMATION REGISTER ADC: HOW TO IMPROVE THEM - 2



Charging capacitors:

- Requires energy
- Wastes energy, when done <u>resistively</u> from $V_{\underline{start}}$ to $V_{\underline{end}}$

So: we're doing something else



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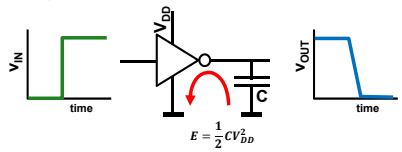

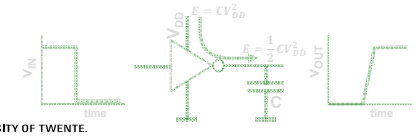

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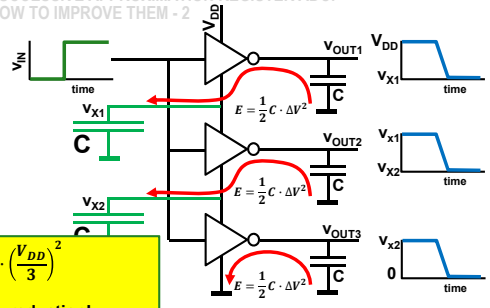
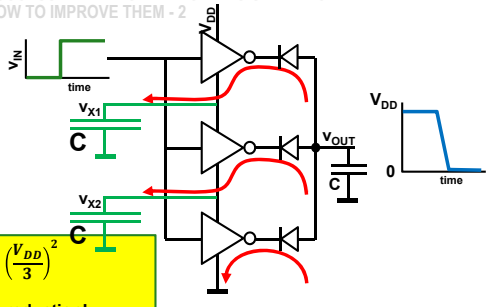


$E = 3\frac{1}{2}C \cdot \left(\frac{V_{DD}}{3}\right)^2$

3x energy reduction!

SUCCESSIVE APPROXIMATION REGISTER ADC: HOW TO IMPROVE THEM - 2



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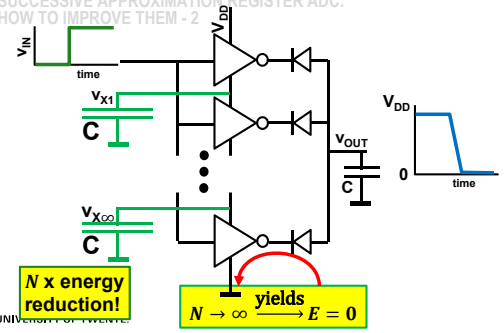

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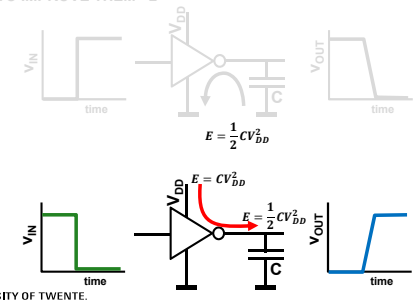

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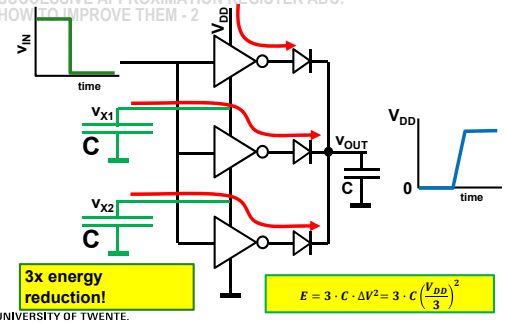

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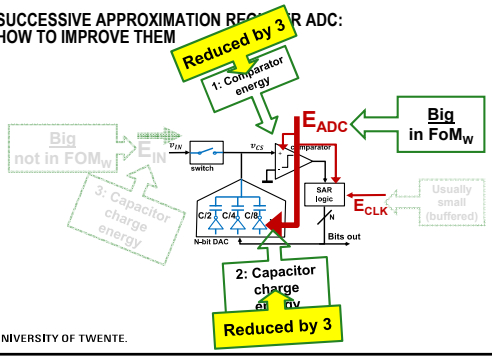
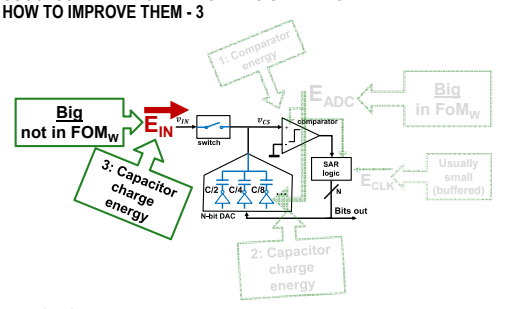


SUCCESSIVE APPROXIMATION REGISTER ADC: HOW TO IMPROVE THEM - 3



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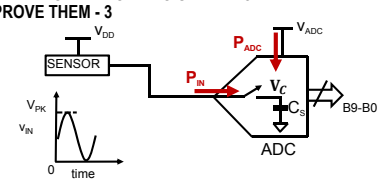
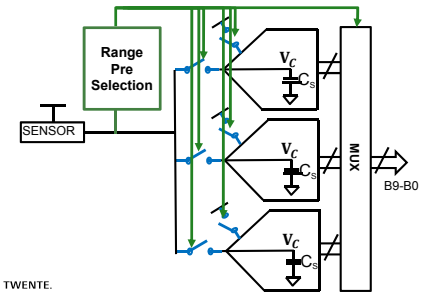


- For state-of-the-art FoM$_W$ ADC [Hsieh, VLSI 2016], P_{ADC} = 0.2µW.
- However, $P_{IN,fundamental} = C_S \cdot V_{PK}^2 \cdot f_S$
  - **Not included in FoM$_W$**
  - **Estimated: ~30x P_{ADC}**

SUCCESSIVE APPROXIMATION REGISTER ADC: HOW TO IMPROVE THEM - 3



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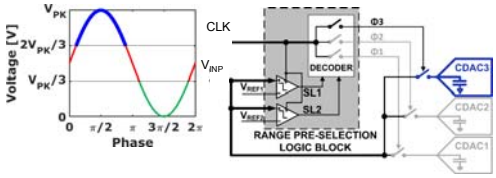

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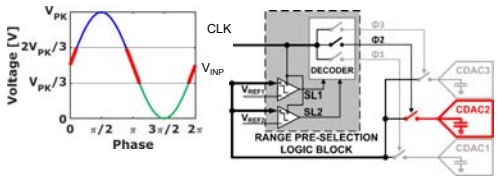

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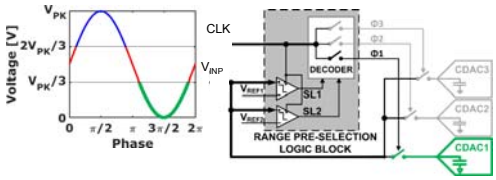

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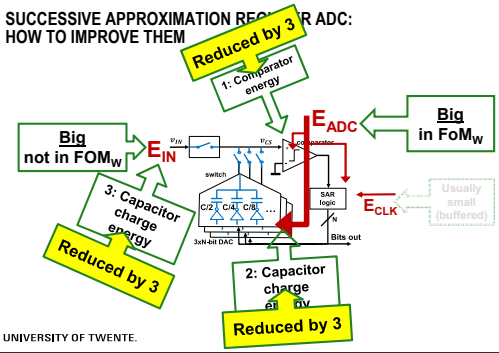
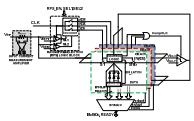
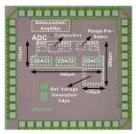
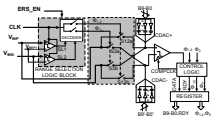


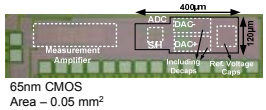
SUCCESSIVE APPROXIMATION REGISTER ADC: MEASUREMENTS





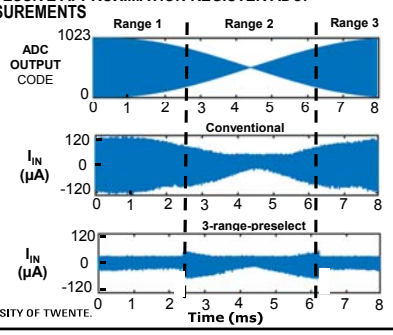
65nm CMOS
Area – 0.08 mm²
(including decaps)





65nm CMOS
Area – 0.05 mm²
(including decaps)

SUCCESSIVE APPROXIMATION REGISTER ADC: MEASUREMENTS



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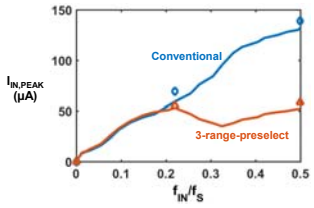
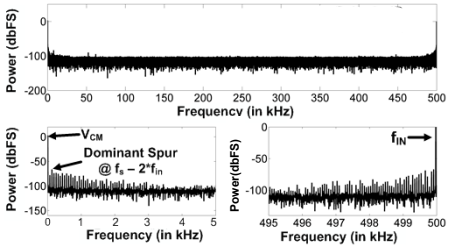


- **Input Current Measurement**
  - **Peak input current reduced > factor 2.4**

SUCCESSIVE APPROXIMATION REGISTER ADC: MEASUREMENTS

- **FFT (Range Pre-Selection Sampling)**



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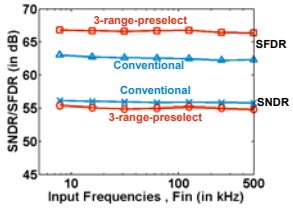


- **SNDR/SFDR v/s f_{IN}**
  - **Reduced voltage swing across S/H switches: better SFDR**

SUCCESSIVE APPROXIMATION REGISTER ADC: MEASUREMENTS

Architecture	This Work		[1]	[2]	[3]	[4]
	SAR with MES	SAR with CS				
Technology	65nm	65nm	40nm	40nm	65nm	90nm
Resolution[bits]	10	10	11	10	10	10
Supply [V]	1	1	0.3	0.45	0.6	0.7
Maximum Sampling Rate	1 MS/s	1 MS/s	600 kS/s	200 kS/s	40 kS/s	4 MS/s
Ideal Input Swing, V_{FS} [V]	2	2	1.2	0.9	1.2	1.4
ADC Energy, E_{ADC} (in pJ)	3.2	3.2	0.312	0.42	1.8	3
E_{SNDR} (in pJ), Linear settling, theoretical minimum*	3.65	8.4	9.41	9.53	20.6	70
ENOB [bits]	9.07	9.17	9.46	8.75	9.4	9.05
FoM_s (fJ/conversion)	5.9	5.5	0.44	0.85	2.2	5.2
$FoM_{W,rN}$ (fJ/conversion)* @Nyquist	13.8	21	27.2	26	33.2	125

[1] S.-E. Haleh et al., "A 0.44fJ/conversion-step 11b 600kS/s SAR ADC with Semi-resiting DAC", *VLSI Symposium 2016*.
[2] Hong-Yen Tai et.al, "A 0.85fJ/conversion-step 10b 200kS/s subranging SAR ADC in 40nm CMOS", *ISSCC 2014*.
[3] P. Harpe, et al., "A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction", *ISSCC 2013*.
[4] C. Y. Liou et. al, "A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with charge-average switching DAC in 90nm CMOS," *ISSCC 2013*.

CONTENTS

- University of Twente
- Electrical Engineering
- IC-Design group

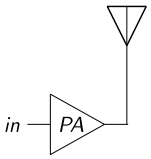
- **Some examples of circuit innovation**
  - Intro
  - How to improve SAR ADC performance
  - **Class-E RF power amplifiers**
  - Wrap up

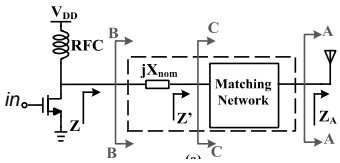
CLASS-E RF POWER AMPLIFIERS

- Some metrics
  - RF power
  - Efficiency
  - Robustness
  - ~~Modulation~~
- Higher efficiency
  - Class A
  - Class E
  - Outphasing class E
- Self-healing

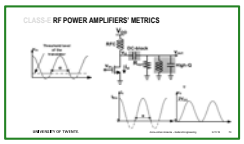
CLASS-E RF POWER AMPLIFIERS' METRICS

- Class A-B-C



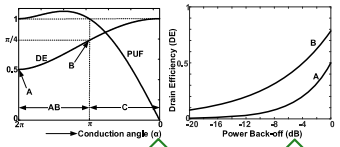


CLASS-E RF POWER AMPLIFIERS' METRICS



Drain Efficiency:

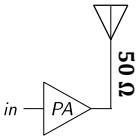
$$DE = \frac{P_{load}}{P_{VDD}}$$

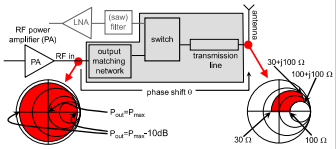


High DE
Low PUF

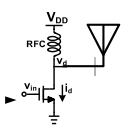
DE
drops quickly

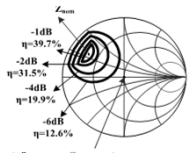
CLASS-E RF POWER AMPLIFIERS' LOAD EFFECTS

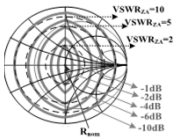


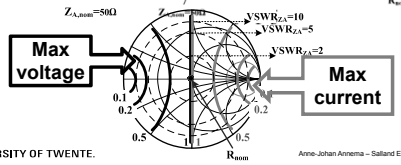


CLASS-E RF POWER AMPLIFIERS' LOAD EFFECTS



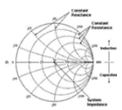






Max voltage

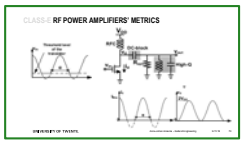
Max current

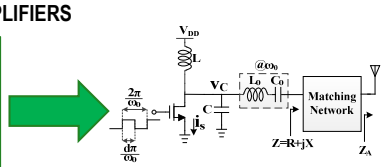


CLASS-E RF POWER AMPLIFIERS

- Some metrics
  - RF power
  - Efficiency
  - Robustness
  - ~~Modulation~~
- Higher efficiency
  - Class A
  - Class E
  - Outphasing class E
- Self-healing

CLASS-E RF POWER AMPLIFIERS





Class A
- **"Linear" modulation (amplitude and phase)**
- **"low" efficiency: overlap V>0 and I>0**

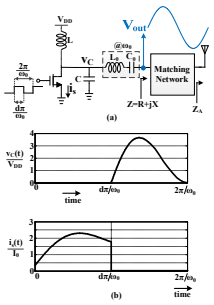
Switched mode PA
- **Class E (here)**
- **Modulation:**
  - **On-off keying**
  - **Phase keying**

CLASS-E RF POWER AMPLIFIERS

Ideal class E PA:
- **Z**ero **V**oltage **S**witching
- **Z**ero **S**lope **S**witching

$$\begin{cases} V_C\left(\frac{2\pi}{\omega}\right) = 0 \\ \frac{dV_C}{dt}\left(\frac{2\pi}{\omega}\right) = 0 \end{cases}$$

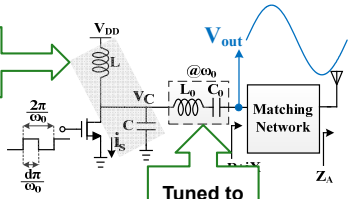
- Only {L, C, switch} in the PA



CLASS-E RF POWER AMPLIFIERS

Tuned to do ZVS + ZSS

"sees" Z_A



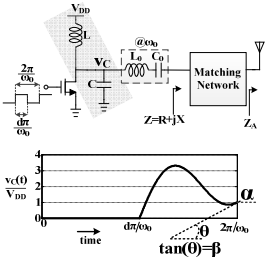
Tuned to $f_{transmit}$

CLASS-E RF POWER AMPLIFIERS

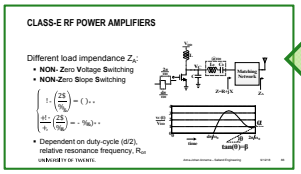
Different load impendance Z_A:
- **NON- Z**ero **V**oltage **S**witching
- **NON-Z**ero **S**lope **S**witching

$$\begin{cases} v_c\left(\frac{2\pi}{\omega_0}\right) = \alpha V_{DD} \\ \frac{dv_c}{dt}\left(\frac{2\pi}{\omega_0}\right) = \beta\omega_0 V_{DD} \end{cases}$$

- Dependent on duty-cycle (d/2), relative resonance frequency, R_{on}



CLASS-E RF POWER AMPLIFIERS

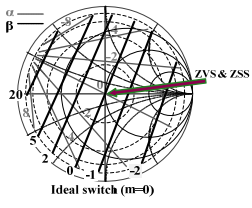


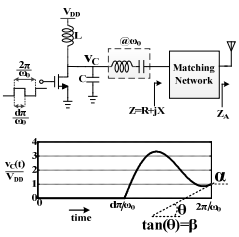
ZVS and ZSS: 100% DE

Non-ZVS Non ZSS: So what???

CLASS-E RF POWER AMPLIFIERS: LOAD MISMATCH

- Nominal at ZVS and ZSS (q=1.412 , d=1: max power)





CLASS-E RF POWER AMPLIFIERS: LOAD MISMATCH

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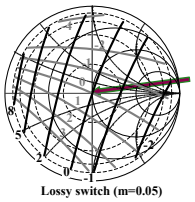
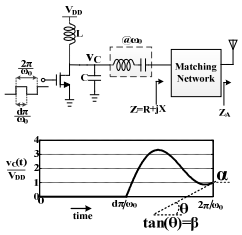
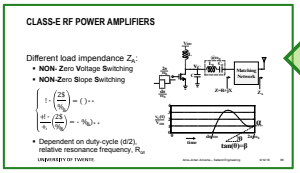


Lossy switch (m=0.05)



CLASS-E RF POWER AMPLIFIERS



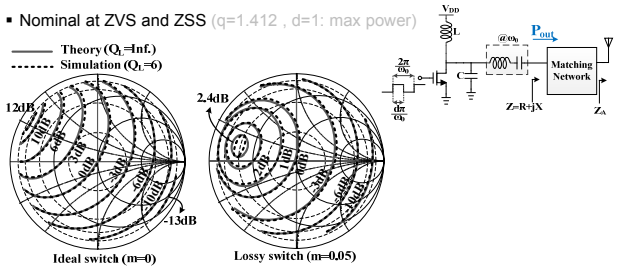
ZVS and ZSS: 100% DE

Non-ZVS Non ZSS: So what???

Impact on DE and P_{out}

CLASS-E RF POWER AMPLIFIERS: LOAD MISMATCH → P_{OUT}

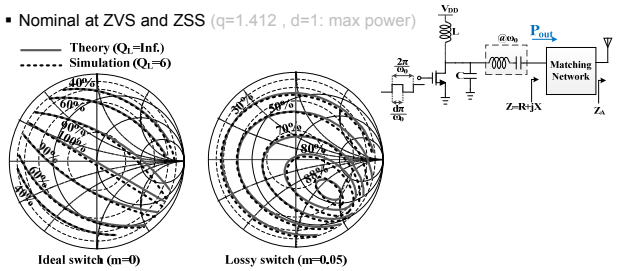
- Nominal at ZVS and ZSS (q=1.412 , d=1: max power)



Ideal switch (m=0) Lossy switch (m=0.05)

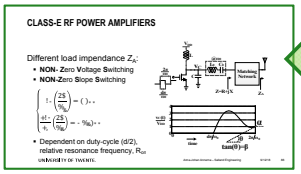
CLASS-E RF POWER AMPLIFIERS: LOAD MISMATCH → DE

- Nominal at ZVS and ZSS (q=1.412 , d=1: max power)



Ideal switch (m=0) Lossy switch (m=0.05)

CLASS-E RF POWER AMPLIFIERS



ZVS and ZSS: 100% DE

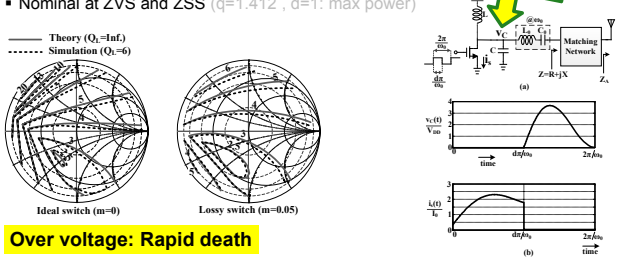
Non-ZVS Non ZSS: So what???

Impact on reliability

CLASS-E RF POWER AMPLIFIERS: LOAD MISMATCH → RELIABILITY

V_C/V_{DD}

- Nominal at ZVS and ZSS (q=1.412 , d=1: max power)

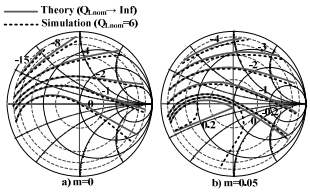


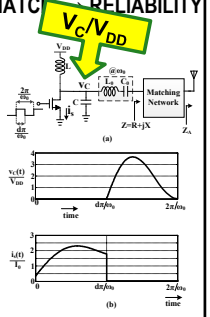
Ideal switch (m=0) Lossy switch (m=0.05)

Over voltage: Rapid death

CLASS-E RF POWER AMPLIFIERS: LOAD MISMATCH → RELIABILITY

- Nominal at ZVS and ZSS (q=1.412 , d=1: max power)

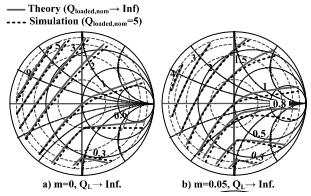


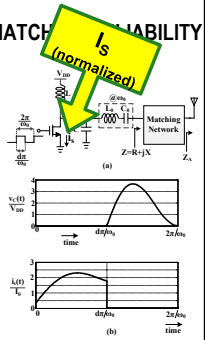


Under voltage: Rapid death

CLASS-E RF POWER AMPLIFIERS: LOAD MISMATCH → RELIABILITY

- Nominal at ZVS and ZSS (q=1.412 , d=1: max power)

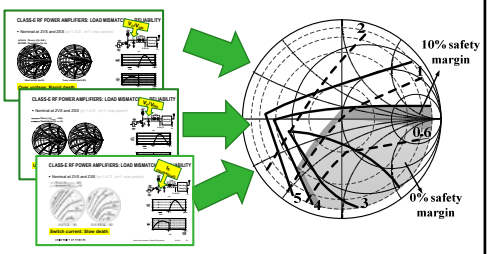




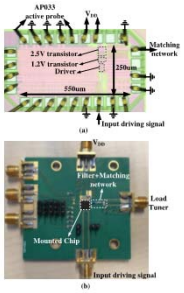
Switch current: Slow death

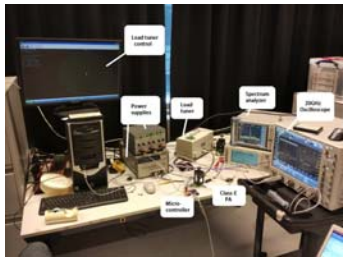
CLASS-E RF POWER AMPLIFIERS: LOAD MISMATCH → SOA

- Nominal at ZVS and ZSS (q=1.412 , d=1: max power)
- V_{cmax}<$V_{cmax,n}$
- I_{smax}<$I_{smax,n}$



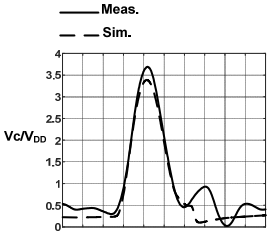
CLASS-E RF POWER AMPLIFIER





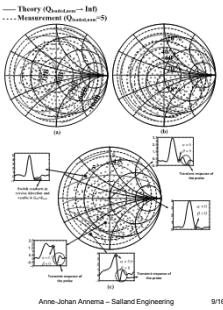
CLASS-E RF POWER AMPLIFIERS

- f=1.4 GHz, V_{DD}=1.15V
- **Results: nominal Load**
- Pout
  - Measured: 64mW
  - Simulated: 62mW
- Efficiency
  - Measured: 71%
  - Simulated: 70%

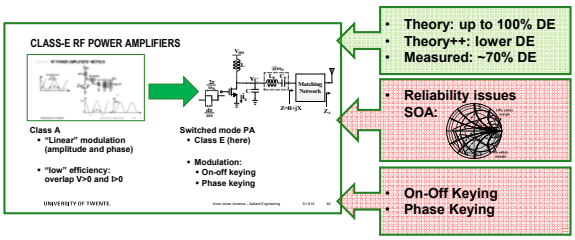


CLASS-E RF POWER AMPLIFIERS

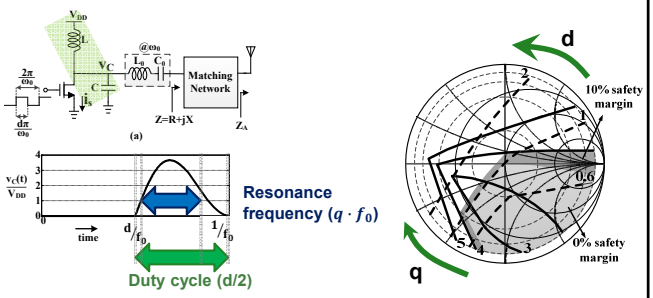
- **Load pull results:**
- At nominal Load:
  - Pout
    - Measured: 64mW
    - Simulated: 62mW
  - Efficiency
    - Measured: 71%
    - Simulated: 70%



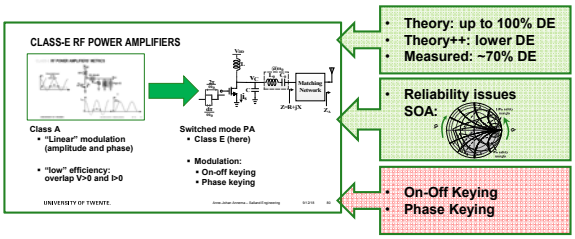
CLASS-E RF POWER AMPLIFIERS



CLASS-E RF POWER AMPLIFIERS: SOA SOLUTIONS



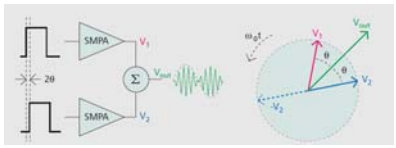
CLASS-E RF POWER AMPLIFIERS



CLASS-E RF POWER AMPLIFIERS: OUTPHASING

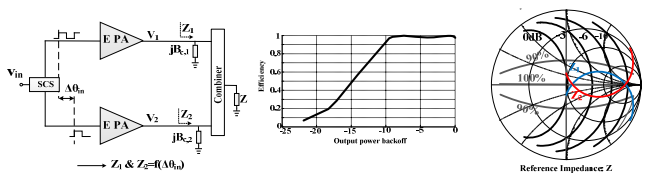
Linear amplification by nonlinear component(LINC) [1]

- Amplitude information → phase information
- Amplification by efficient nonlinear PA
- Phase information → Amplitude information: Power combiner

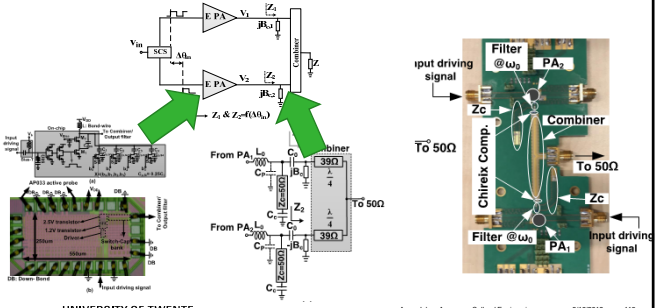


de Vreede, L.C.N.; Acar, M.; Calvillo-Cortes, D.A.; van der Heijden, M.P.; Wesson, R.; de Langen, M.; Qureshi, J., "Outphasing transmitters, enabling digital-like amplifier operation with high efficiency and spectral purity," Communications Magazine, IEEE , vol.53, no.4, pp.216,225, April 2015

CLASS-E RF POWER AMPLIFIERS: OUTPHASING



CLASS-E RF POWER AMPLIFIERS: OUTPHASING



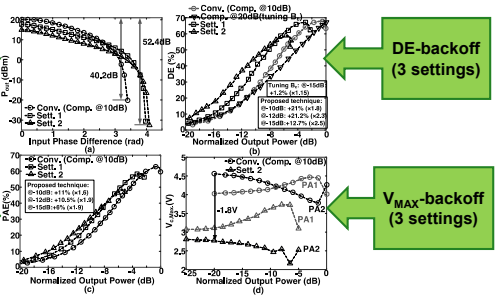
CLASS-E RF POWER AMPLIFIERS: OUTPHASING

Adjustable power level (3 settings)

PAE-backoff (3 settings)

DE-backoff (3 settings)

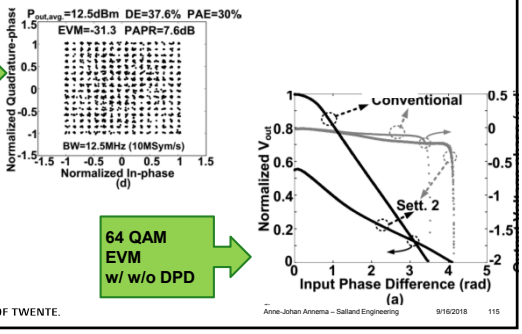
V_{MAX}-backoff (3 settings)



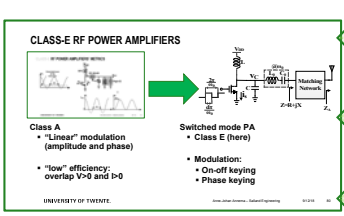
CLASS-E RF POWER AMPLIFIERS: OUTPHASING

PSD @ 64 QAM @ 1.8 GHz

64 QAM EVM w/ w/o DPD



CLASS-E RF POWER AMPLIFIERS



- Theory: up to 100% DE
- Theory++: lower DE
- Measured: ~70% DE

- Reliability issues SOA:

- On-Off Keying
- Phase Keying
- Amplitude modulation
- Complex modulations

CONTENTS

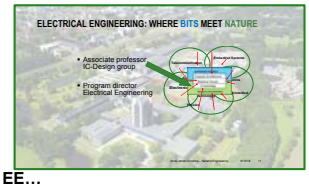
- University of Twente
- Electrical Engineering
- IC-Design group

- **Some examples of circuit innovation**
  - Intro
  - How to improve SAR ADC performance
  - Class-E RF power amplifiers
  - **Wrap up**

WRAP UP

Only small part of:

- **What we do at the University of Twente**
  - **At Electrical Engineering**
    - **At my specific research field in EE…**
      - **Ultra low power SAR ADCs**
      - **Efficient & Robust RF PAs**
      - References
      - Optical stuff in CMOS
      - High speed DAC
      - Fundam…
      - … and h…



Pushing the state-of-the-art in Electrical Engineering

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