MASER
ENGINEERING

Current and Future Q&R testing

SE Opening Symposium – Zwolle, 13-14 September 2018

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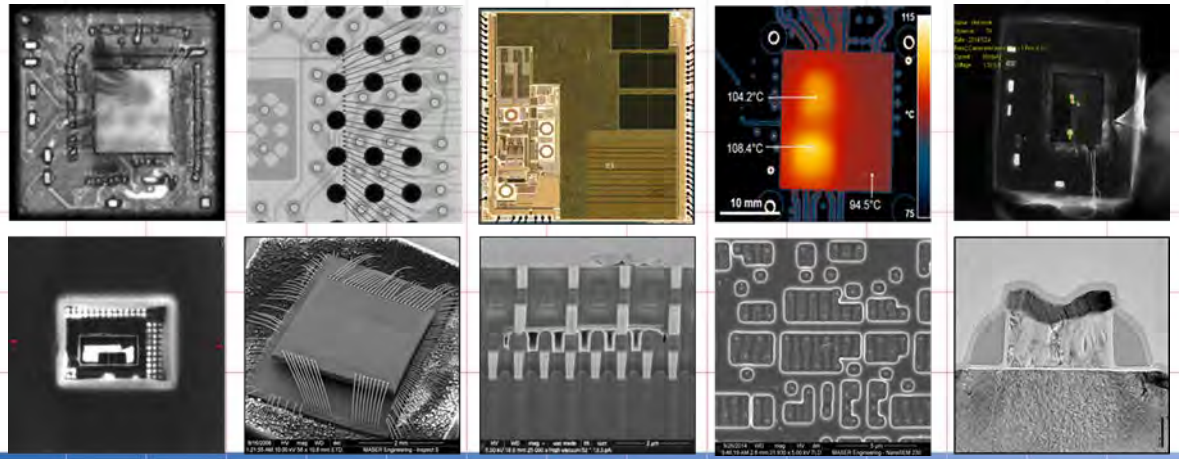
Introduction of MASER Engineering

- Dutch based Independent Service Provider
- Advanced Failure Analysis capabilities
- Full Reliability Testing with wide range of test equipment
- 48 well trained and experienced employees in Test and Analysis
- ISO 17025 accredited and ISO 9001 certified Lab
- Representations covering the EMEA area
- 25 years active since 1993
- Proprietary database system with customer secured project access
- 2100 m^2 office and EPA test and analysis laboratories in NL
- ~150 active customers in Semiconductor IC and components
- ~80 active customers in OEM / system applications

Introduction of MASER Engineering

- **Physical Analysis scope**
  - Non Destructive Analysis: E-test | 2D-XRAY | 3D-XRAY | SAM | LIT | EOTPR
  - Sample Preparation: mechanical grinding & polishing | plasma | FIB
  - Fault Localization: LIT | EMMI | OBIRCH | LVx | C-AFM
  - Imaging & Material Analysis: Optical | SEM | TEM | FIB | AFM | SIMS/Auger*
  - First Silicon Circuit Edit service > 28nm, Front and Backside, CAD driven



Introduction of MASER Engineering

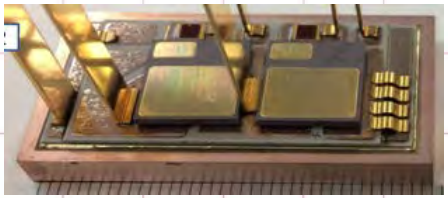
- **Reliability Test scope**
  - Design and Manufacturing of R/T boards and mechanical test fixtures
  - Electrical Test: DC + optical parametric | Structural | ATE | more
  - ESD & Latch-Up test: HBM | MM | CDM | TLP | system
  - Environmental test: HTOL | THB | HAST | TCY | MSL | PTC | more
  - Mechanical test: Vibration | Shock | Centrifuge | Bending | Pull/Shear | more

IC qualification programs

- **Current Standards**
  - Application driven, various severity levels
  - Industry Council driven standardization committees
  - End user specific requirements, custom procedures

- **Generic Standards for the Semiconductor industry**
  - JEDEC, AEC, IEC, ISO, ESDA, DIN, JIS, IPC, MIL, ESCC and more
  - Mix of generic procedures, application specific and detailed test descriptions
  - Inter laboratory correlation programs

- **Extensions for non-IC products**
  - Active (power) semiconductors
  - Passive components
  - System in Package / Modules



IC qualification program JESD-47

- Stress-Test-Driven Qualification of Integrated Circuits
  - Chip and Package related tests
  - 3 lots of ~1.400 IC's each

Table 1 — Device qualificatio

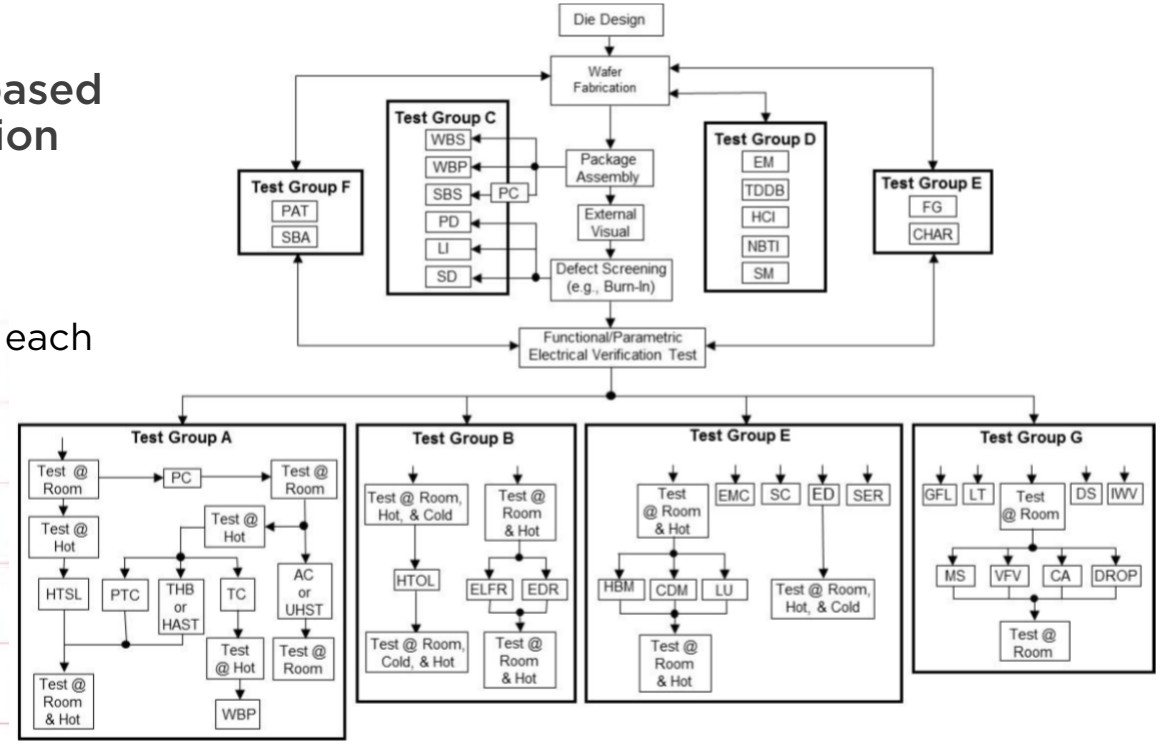
Stress	Ref.	Abbv.	Conditions
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	$T_J \geq 125$ °C $V_{cc} \geq V_{cc}$ max
Early Life Failure Rate	JESD22-A108, JESD74	ELFR	$T_J \geq 125$ °C $V_{cc} \geq V_{cc}$ max
Low Temperature Operating Life	JESD22-A108	LTOL	$T_J \leq 50$ °C $V_{cc} \geq V_{cc}$ max
High Temperature Storage Life	JESD22-A103	HTSL	$T_A \geq 150$ °C
Latch-Up	JESD78	LU	Class I or Class II
Electrical Parameter Assessment	JESD86	ED	Datasheet
Human Body Model ESD	JS-001	ESD-HBM	$T_A = 25$ °C
Charged Device Model ESD	JS-002	ESD-CDM	$T_A = 25$ °C
Accelerated Soft Error Testing	JESD89-2, JESD89-3	ASER	$T_A = 25$ °C
"OR" System Soft Error Testing	JESD89-1	SSER	$T_A = 25$ °C

Table 2 — Qualification tests for components in nonhe

Stress	Ref.	Abbv	Conditions
MSL Preconditioning Must be performed prior to: THB, HAST,TC, AC, & UHAST	JESD22 -A113	PC	Per appropriate MSL level per J-STD-020
High Temperature Storage[1]	JESD22 -A103 & A113	HTSL	150 °C + Preconditioning if Required
Temperature[2] Humidity bias (standard 85/85)	JESD22 -A101	THB	85 °C, 85 % RH, V_{cc} max
Temperature[2,3] Humidity Bias (Highly Accelerated Temperature and Humidity Stress)	JESD22 -A110	HAST	130 °C / 110 °C, 85 % RH, V_{cc} max
Temperature Cycling	JESD22 -A104	TC	B[4] -55 °C to +125 °C G[4] -40 °C to +125 °C C[4] -65 °C to +150 °C K[4] 0 °C to +125 °C J[4] 0 °C to +100 °C
Unbiased Temperature/Humidity (Unbiased HAST[3])	JESD22 -A118	UHAST	130 °C / 85% RH 110 °C / 85% RH
Unbiased Temperature/Humidity (Autoclave[5])	JESD22 -A102	AC	121 °C / 100% RH
Solder Ball Shear	JESD22 -B117	SBS	Characterization
Bond Pull Strength[7]	M2011	BPS	Characterization, Pre Encapsulation
Bond Shear[7]	JESD22 -B116	BS	Characterization, Pre Encapsulation
Solderability	M2003 J-STD-002	SD	Characterization
Tin Whisker Acceptance	JESD22 -A121 through rqmts of JESD 201	WSR	Characterization per JESD201

IC qualification program AEC-Q100

- Failure Mechanism based stress test qualification for IC's
  - Severity grade 0-4
  - 7 test groups
  - 3 lots of ~1.400 IC's each



IC qualification

- **Way of Working**
  - Device specification
  - E-test definition → choise of ATE
  - Characterization program definition
  - H/W for ATE test, ESD/LU, Operating Life, HAST, BLRT and mech tests
  - Application and mission profile → severity grade
  - Qualification program definition
  - Qualification lot IC manufacturing
  - Wafer lot related tests
  - Qualification lot IC packaging, including BLRT daisy chain samples
  - Execution of qualification program including readpoint E-test
  - Data processing and review
  - Failure Analysis including E-FA, NDA and P-FA
  - Final qualification report and device release

Si-CMOS IC Technology impact

- CMOS advanced nodes to 7/10nm FinFET
- Very high pin count interconnect
- Ultra high data rates
- Low core voltages
- ESD sensitivity

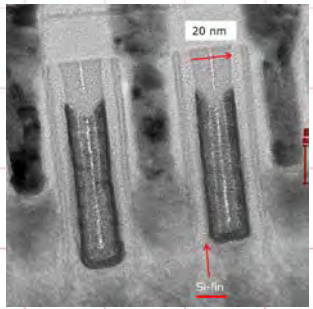
IMEC LOGIC DEVICE ROADMAP

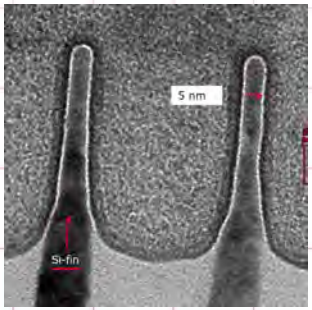
DEVICE TECHNOLOGY FEATURES

Early production	2013 - 2014	2015 - 2016	2017 - 2018	2019 - ...
	16 -14nm	10nm	7nm	5nm
Vdd (V)	0.8	0.8-0.7	0.7-0.5	0.7-0.5
	Planar SOI / Bulk FinFET	SOI FinFET / SiGe/Ge channel	IIIV channel / Lateral Nanowire	Vertical Nanowire
Device	FinFET (Bulk, SOI), FDSOI	FinFET (Bulk, SOI)	FinFET (GAA, QW, SOI)	GAA lateral NW; (Vert. NW)

Improve Electrostatics

- Impact on
  - ATE solutions → interconnect and speed
  - Operating Life Test solutions → power handling
  - ESD Test levels → lower resistance voltage
  - Electrical FA → use of BIST and Scanpath
  - Failure Analysis → dynamic fault localization

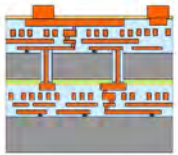
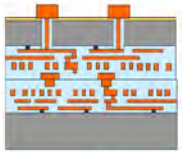
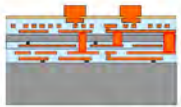
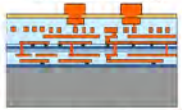




3D Packaging Technology impact

3D TECHNOLOGY LANDSCAPE

imec

	3D-SIC	3D-SOC			3D-IC
wiring level	Global	Semi-global	Intermediate	Local	FEOL
2-tier stack				2nd FEOL after stacking 	Multi-tier FEOL 
Contact Pitch *Relative density:*	40 ⇒20 ⇒10 ⇒*5µm* 1/16⇒¼ ⇒1 ⇒ 4	5 ⇒ 1 µm 4 ⇒ 100	2 µm ⇒ 0.5 µm 50 ⇒ 400	200 ⇒ 100 nm 5000 ⇒ 10000	< 100 nm > 10000
Partitioning	Die	**blocks** of standard cells		**Gates**	**Transistors**

- **Impact on**
  - Device handling → Brittle material
  - Test socket interconnect → Fine pitch limits
  - Failure Analysis → Demounting techniques/tools
  - Defect models → New material behavior

Other materials / application impact

- 5G & IoT applications
- GaN (RF) power devices
- MEMS devices
- III-V optical materials

- Impact on
  - E-Test solutions → RF to optical, mechanical or chemical interaction
  - Qualification setup → Unknown failure mechanisms for stress acceleration
  - Foreign E&M exposure → Conversion testing of E&M response to E-test
  - Power handling solutions → High Current and Power handling during on state
  - Failure Analysis → New materials and constructions

New developments in Q&R programs

- **Q&R program definition**
  - Application driven, various severity levels
  - New IC technology → new wearout mechanisms require new methods
  - New packaging technology → interconnection testing becomes vital
  - Industry Council driven standardization committees → influence the working practise
  - End user specific requirements, custom procedures based on mission profiles

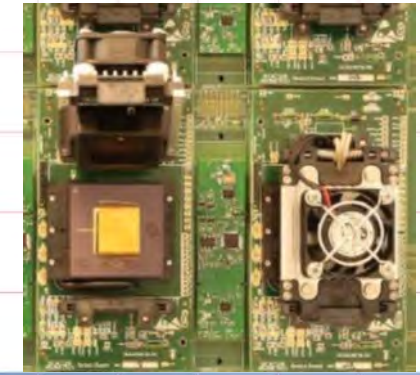
- **Pre qualification activities**
  - Design stable setup modes and BIST during HTOL
  - Concurrent engineering during IC and Package design/definition
  - BLR test on assembly technology based on Daisy Chain device
  - Sample preparation feasibility
  - Materials evaluation and de-processing development

New developments in Q&R programs

- **ESD & Latch-Up Standards for the Semiconductor industry**
  - Joint standard effort of ESDA and JEDEC
  - ANSI/ESDA/JEDEC JS-001:2017 for HBM (replacement of JS-001:2014)
    - Lower minimum HBM ESD stress voltage levels: 2kV → 500V
    - Improved multi powergroup combination testing to avoid overstress wearout
    - Statistical approach of multiple I/O circuits accepted
  - ANSI/ESDA/JEDEC JS-002-2014 for CDM (revision JS-002-2017pending)
    - AEC-Q100-011-C1 automotive CDM standard → joining JS-002 under discussion
  - New HMM method under development to replace IEC61000-4-2 system test standard
    - Current standard is for systems, not IC's
    - New Human Metal Model now at Standard Practice level, Round Robin tests pending
    - Simulating galvanic path from IC to output connector
    - Standardization co-chaired by MASER Engineering
  - Latch-Up standard JESD-47E:2016 to be revised to JESD-47F
    - Major update since current version does not adapt current I/O designs very well

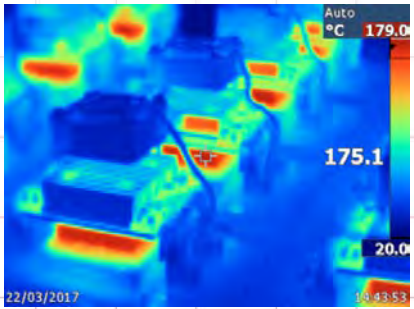
New tools for Q&R programs

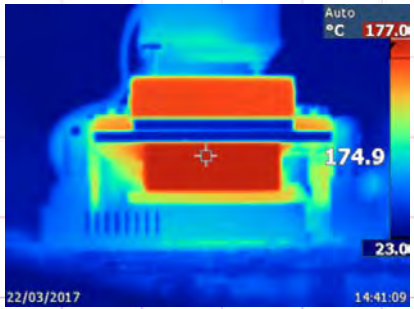
- **High/Low Temperature Operating Life testing device testing**
  - Sub 20nm FINFET with increasing process variation impact → thermal run-away
  - High pincount devices as flip-chip BGA or LGA packages → square board style
  - High speed data busses and serial control busses → SPI and STIL vector conversion
  - Multiple Low Voltage / High Current power supply connections → multiple PS control
- **Evaluation unit of new HTOL system**
  - Debug station with 1:1 BIB and driver of Synergie CAD UDx-700

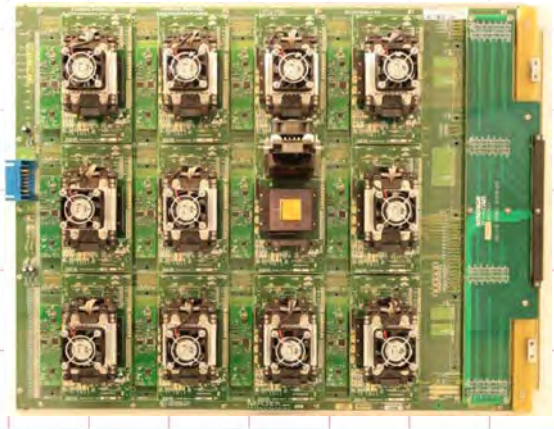


New tools for Q&R programs

- **Thermal package control**
  - Individual heater + heatsink + fan, build on socket module
  - Active case temperature sensor and controller with interface to BI-system controller
  - Avoid thermal run-away due to process variations at sub-20nm FF nodes
  - Balance junction temperature over test lot for proper thermal modelling statistics
  - Allows additional circuitry on socket module within normal operating temperatures







New tools for Q&R programs

- 2 temperature zones, -20°C to +170°C, 12 BiB per zone
- 65 power controllers per driver/BiB, up to 248 Amp

Power Supply Module	Voltage Range	Max Current	Power	Precision
UDPSA-12-5-P	0.6/12.0 V	5 A	60 W	5mV/1%
UDPSA-12-10-P	0.6/12.0 V	10 A	120 W	5mV/1%
UDPSA-12-20-P	0.6/12.0 V	20 A	240 W	5mV/1%
UDPSB-15-5-P	0.6/15.0 V	5 A	75 W	5mV/1%
UDPSC-100-40-P	15.0/100.0 V	2.6 A	40 W	150mV/1%
UDGPSA&B-12-5-P	0.6/12.0 V	5 A	60 W	5mV/1%
UDGPSD-12-5-N	-12.0/-0.6 V	5 A	60 W	5mV/1%
UDBPSA&B&C-15-5-P	0.6/15.0 V	5 A	75 W	5mV/1%
UDGREFA&B&C&D-10-02-P-N	-10/10 V	0.2 A	2W	5mV/1%

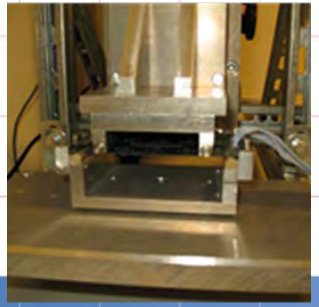
- 450x580mm BiB with fine pitch socket modules (daughter cards)

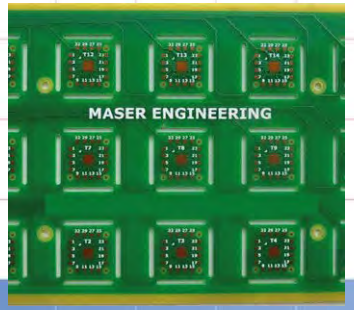
New tools for Q&R programs

- **320 channels**
  - tristate per 16ch
  - clock 20 MHz (50 to 500 MHz upon request)
  - > 100Mb deep pattern through SSD on each driver
- **24 on-board function generators**
  - Sine/Square/AWG, also analog voltage monitoring
- **Protocol communication with on-board µC**
  - SPI, I^2C, JTAG, UART, etc.
  - Custom protocols can be defined
- **Intuitive software**
  - Smart recipe management and compilation
  - Pattern development and import (STIL, WGL, VCD…)
  - Webbased software for monitoring

New tools for Q&R programs

- **Board Level Reliability Test**
  - Mechanical stress test of complex interconnects in package
  - Daisy chain interconnection from external balls to chip
  - Glitch detection on DC resistance of daisy chain
  - SAM, CT-XRAY and Xsie defect monitoring
- **Tool impact**
  - Drop test equipment
  - Bending tool
  - Slow TCY with monitoring





Summary

- New developments in Semiconductor Technology have impact on device behavior during stress tests
- Both advanced IC and Package manufacturing introduce new materials, constructions and therefore new failure mechanisms
- Complexity of (ATE) test program and qualification program meets with design complexity
- Challenges also in new test instrument as well as stress tools design
- Split complex construction in separate stress tests in order to keep a clear view on the various failure mechanisms
- Support actively the standardization committees in order to have a working practise that meets with state-of-art design and manufacturing capabilities