APPLICOS
a SALLAND Engineering Company

PA72 Series

PXI/PXIe Generator & Digitizer platform

PXI™

PXI Express™

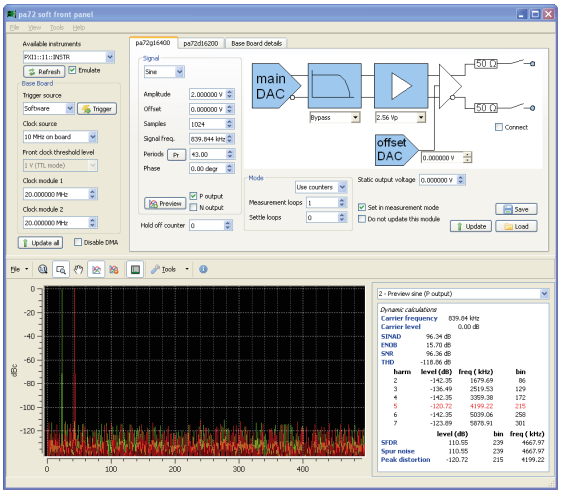
Features

- Flexible analog signal generation and capture platform
- Two daughter board slots
- Choose daughter boards from the 7 available types
- On-board high accuracy voltmeter
- On-board high performance clock source
- 1ppm clock stability / 0.5ps clock jitter
- Available for PXI and PXI Express
- LabView and LabWindows/CVI (VXIplug&play compatible) drivers included

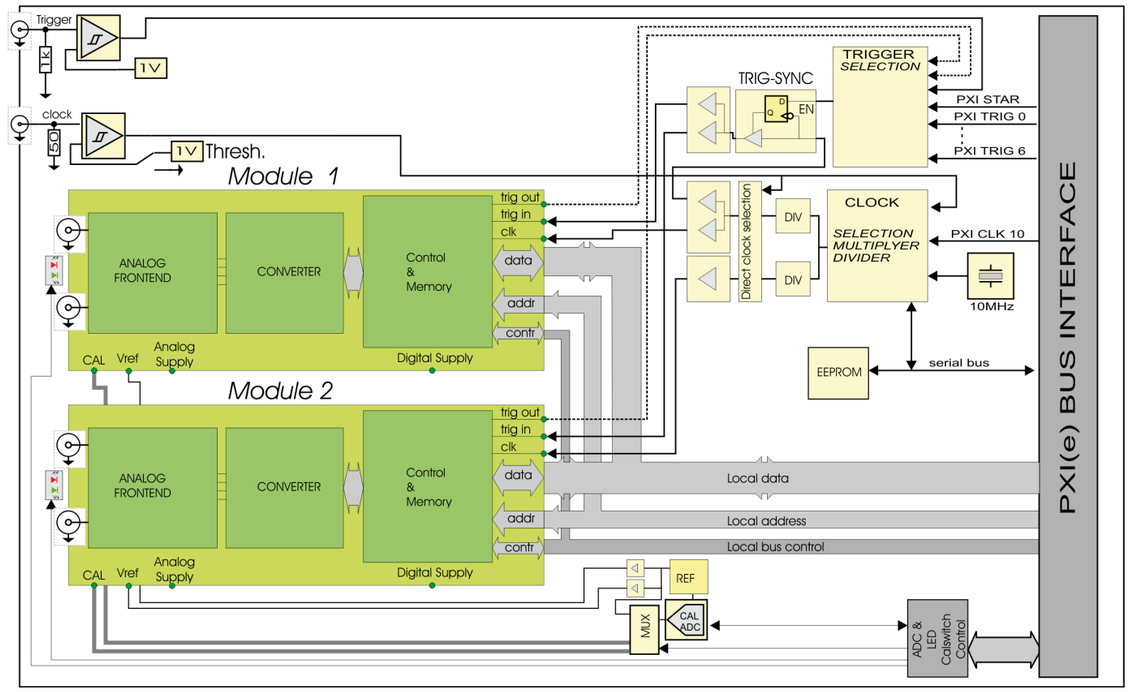
General description

The PA72 platform is a platform of flexibility. It consists of a base board and one or two daughter boards. In daughter boards there is choice from several different generators, digitizers, filters, and Flexible Digital I/O modules. Also custom daughter boards can easily be created. This allows you to configure a data acquisition card exactly tailored to your needs. The PA72 concept provides a flexible and cost effective solution for medium and high end analog functions. Each daughter board is optimized for best signal performance. A PA72 daughter board typically has Differential In-/Outputs, Low THD, Low Noise and High Accuracy. The base board contains a 2-channel high-stability and low-jitter PLL clock generator, trigger circuitry, and of course the PXI-bus interface. A digital voltmeter is available for self-calibration purposes (supported by the driver), and can also be used for custom development boards.

The base board is available with PXI bus interface (PA72) and PXI-Express bus interface (PA72e). Both baseboards accept the same daughter boards. The J2 connector is a small version (XJ4) to ensure both versions are hybrid-slot compatible.



User control panel for the PA72 and an AWG daughter board



Block diagram

PA72 Base board

The PA72 base board contains a clock generator, trigger circuitry, a digital voltmeter and the PXI bus interface. In the block diagram below, the base board functions are yellow and the daughter board functions are green.

The clock generator is a low jitter PLL clock that has less than 0.5ps jitter for low loop filter bandwidths. With higher loop filter bandwidths, frequency settling time can be less than 250ms.The main clock frequency ranges from 2kHz up to 945MHz with a resolution of less than 1 kHz. Each daughter board slot has its own clock divider. Therefore the clock for each daughter board can be different while maintaining proper synchronization.

The PLL clock generator features a high stability, low noise and low jitter 10MHz onboard reference clock with 1ppm frequency stability. In addition the PLL can be locked to the PXI backplane clock or to an external reference clock. The on-board clock source can also be bypassed by an external direct clock.

The trigger input supports edge and level triggering and positive and negative going trigger signals. The trigger source can be software, PXI Star trigger, PXI Trigger 0-6, or external (front). Additionally, digitizer boards can be set to edge-trigger on the analog input signal.

Specifications

PLL clock

Frequency range	2kHz to 945MHz
Sync possibilities	10MHz backplane or 10MHz external clock
PLL lock time	250ms - 1s (depending on loop ilter BW)
Jitter	0.5ps typical

External clock input

Clock rate	DC to 500MHz
Threshold level	0V or 1V (programmable)
Input impedance	50 Ohm

Front trigger input

Threshold level	1V
Input impedance	1k Ohm
Max input level	-0.5V to +5.5V
Coupling	DC

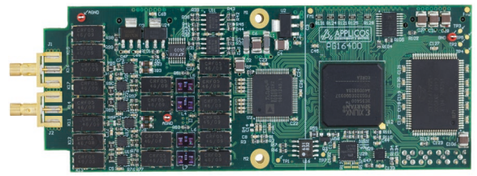
Trigger sources

Digitizer's analog level trigger, Front trigger input, PXI STAR, PXI TRIG 0..6 (3..6 inverted), Software trigger

Bus interface

PA72 bus	32-bit PXI, burst mode support
PA72e bus	x1 PXI Express, burst mode support
Max. burst data rate	132 MByte/s

PA72G16400 daughter board 16-bit / 400Msps Arbitrary Waveform Generator

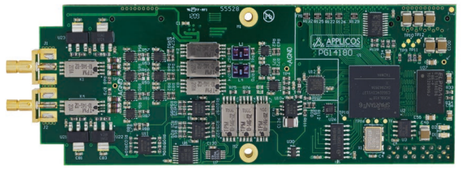


The PA72G16400 is a 16-bit arbitrary waveform generator, capable of generating waveforms at speeds up to 400Msps. The high resolution and the high sample rate allows generating signals with very low quantization noise levels. An onboard offset voltage source allows generating offset signals while maintaining optimal utilization of the DAC's digital range. With the 8MWord of memory, there is lots of room for uploading several different patterns, allowing switching patterns with minimal bus communication.

PA72G16400 Specifications

Channels	1
Resolution	16-bit
Update rate with PA72 clock	2kHz to 400MHz
Update rate external clock	DC to 400MHz
Pattern depth	8M-words
Output ranges Single-Ended	0.32VP to 2.56VP in 6 ranges
Output ranges Differential	0.64VP to 5.12VP in 6 ranges
DC-offset voltage	-2.56 to +2.56V (>14-bit resolution)
Output configuration	50-Ohm, Single-Ended or Differential
Bandwidth	DC to 80-140MHz
Output filters	Bypass, 60MHz, 30MHz
Absolute accuracy (Vout+)	± (250µV + 0.1% of range + 0.1% of value)
Relative accuracy	±0.006%
SNR (200Msps, 5VPP diff.)	69dB @ FOUT = 1MHz (BW 0-80MHz)
SNR (200Msps, 5VPP diff.)	67dB @ FOUT = 10MHz (BW 0-80MHz)
THD (200Msps, 5VPP diff.)	84dB @ FOUT = 1MHz
THD (200Msps, 5VPP diff.)	73dB @ FOUT = 10MHz
SFDR (200Msps, 5VPP diff.)	82dB @ FOUT = 1MHz

PA72G14180 daughter board 14-bit / 180Msps Arbitrary Waveform Generator

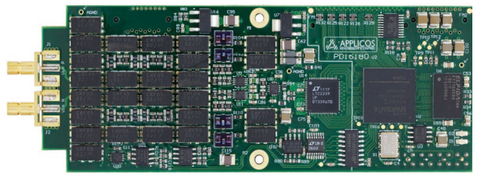


The PA72G14180 is a 14-bit arbitrary waveform generator, capable of generating waveforms at speeds up to 180Msps. An onboard offset voltage source allows generating offset signals while maintaining optimal utilization of the DAC's digital range. With the 64MWord of memory, there is lots of room for uploading long complex waveforms. Also uploading of many different patterns is possible, allowing switching patterns with minimal bus communication.

PA72G14180 Specifications

Channels	1
Resolution	14-bit
Update rate with PA72 clock	2kHz to 180MHz
Update rate with ext. clock	DC to 180MHz
Pattern depth	64M-words
Output ranges	0.2VP to 3.28VP proportional ranging
DC-offset voltage	-2.56V to +2.56V
Output configuration	50-Ohm, Single-Ended or Differential
Bandwidth	DC to 90MHz
Output filters	Bypass, 30MHz, 15MHz
Absolute accuracy	±(250µV + 0.1% of range + 0.1% of value)
Relative accuracy (INL)	±0.025% of range
SNR (180Msps, 3.2VPP diff.)	68dB @ FOUT = 1MHz (BW 0-70MHz)
SNR (180Msps, 3.2VPP diff.)	64dB @ FOUT = 10MHz (BW 0-70MHz)
THD (180Msps, 2.0VPP diff.)	81dB @ FOUT = 1MHz
THD (180Msps, 2.0VPP diff.)	70dB @ FOUT = 10MHz
SFDR (180Msps, 2.0VPP diff.)	82dB @ FOUT = 1MHz
SFDR (200Msps, 5VPP diff.)	82dB @ FOUT = 1MHz

PA72D16180A daughter board 16-bit / 180Msps Digitizer

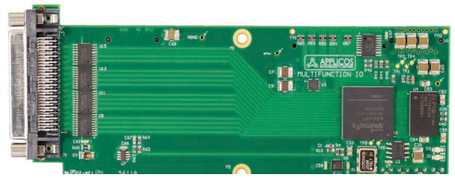


The PA72D16180A is a 16-bit digitizer, capable of capturing waveforms at speeds up to 180Msps. An onboard offset voltage source allows capturing offset signals while still using the optimal range for maximum ADC utilization. Two onboard filters allow suppression of out-of-band noise. The 64MWord onboard memory enables capturing very long waveforms, or sequentially capturing multiple signals with minimal intermediate bus communication.

PA72D16180A Specification

Channels	1
Resolution	16-bit
Sample rate	1MHz to 180MHz
Memory depth	64M-words
Input configurations	50Ω or 1MΩ, AC or DC, Diff. or Single-Ended
Input ranges	50Ω: 0.256VP to 3.072VP in 8 ranges
1MΩ: 0.256VP to 15.36VP in 12 ranges	-2.56V to +2.56V
DC-offset voltage	16-bit resolution
Input bandwidth	DC to 95-170MHz (typical, dep. on range)
Input filters	Bypass, 60MHz, 30MHz
Absolute accuracy (Vin+)	±(250µV + 0.1% of range + 0.2% of value)
Relative accuracy	±0.006%
SNR (180Msps, 50Ω, 4VPP diff)	69dB @ FIN = 1MHz (BW 0-80MHz)
SNR (180Msps, 50Ω, 4VPP diff)	67dB @ FIN = 10MHz (BW 0-80MHz)
THD (180Msps, 50Ω, 4VPP diff)	85dB @ FIN = 1MHz
THD (180Msps, 50Ω, 4VPP diff)	81dB @ FIN = 10MHz
SFDR(180Msps, 50Ω, 4VPP diff)	83dB @ FIN = 1MHz
SFDR (200Msps, 5VPP diff.)	82dB @ FOUT = 1MHz

PA72DIOS6016 daughter board Multifunctional programmable Digital I/O

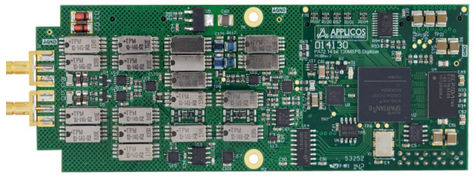


The PA72DIOS6016 is a multifunctional digital design core. The FPGA allows for implementing many different custom applications. The connector has 64 Input/Output pins which can be assigned as TTL I/O or as differential inputs. 128 MByte of DDR2 memory is available to the FPGA, and an onboard EEPROM allows for storing values in non-volatile memory. The I/O bank voltage can be FPGA-selected between 2.5 and 3.3 Volt.

PA72DIOS6016 Specification

FPGA	Xilinx Spartan6 XC6SLX16
Logic cells	14579
CLB Flip-Flops	18224
Front connector	VHDCI SCSI-5
Max. TTL/LVCMOS I/Os	32
Max. differential inputs	32
Max. differential outputs	10
I/O voltages	2.5V and 3.3V
I/O configurations	LVTTL, LVCMOS, PCI, SSTL, (B)LVDS*, LVPECL*, and more.* Differential signals as input only
DDR Memory size	1Gbit
DDR Memory frequency	800MHz
Total block RAM	576kBit
Block RAM max. frequency	320MHz

PA72D14130 daughter board 14-bit / 130Msps Digitizer



The PA72D14130 is a 14-bit digitizer, capable of capturing waveforms at speeds up to 130Msps. An onboard offset voltage source allows capturing offset signals while still using the optimal range for maximum ADC utilization. Two onboard filters allow suppression of out-of-band noise. The 64MWord onboard memory enables capturing very long waveforms, or sequentially capturing multiple signals with minimal intermediate bus communication.

PA72D14130 Specification

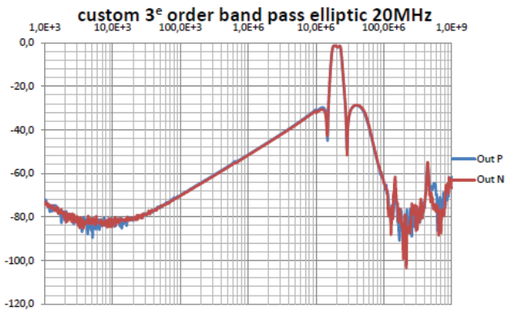
Channels	1
Resolution	14-bit
Update rate with PA72 clock	2kHz to 180MHz
Update rate with ext. clock	DC to 180MHz
Pattern depth	64M-words
Output ranges	0.2VP to 3.28VP proportional ranging
DC-offset voltage	-2.56V to +2.56V
Output configuration	50-Ohm, Single-Ended or Differential
Bandwidth	DC to 90MHz
Output filters	Bypass, 30MHz, 15MHz
Absolute accuracy	±(250µV + 0.1% of range + 0.1% of value)
Relative accuracy (INL)	±0.025% of range
SNR (180Msps, 3.2VPP diff.)	68dB @ FOUT = 1MHz (BW 0-70MHz)
SNR (180Msps, 3.2VPP diff.)	64dB @ FOUT = 10MHz (BW 0-70MHz)
THD (180Msps, 2.0VPP diff.)	81dB @ FOUT = 1MHz
THD (180Msps, 2.0VPP diff.)	70dB @ FOUT = 10MHz
SFDR (180Msps, 2.0VPP diff.)	82dB @ FOUT = 1MHz
SFDR (200Msps, 5VPP diff.)	82dB @ FOUT = 1MHz

PA72BPF daughter board – Dual differential band pass filter

The PA72BPF daughter board is an additional filter board. It typically contains two selectable differential 3rd order elliptic band pass filters. These filter modules are tailored by Applicos to the customers' requirements. The filters can be used to filter the output signal of the generator daughter boards to achieve an even better distortion and noise suppression.

PA72BPF Specifications

Standard values	10 MHz, 20MHz, 35 MHz, 42.5 MHz
Specifications below are typical/indicative values only!	
Pass band	5 MHz
Pass band attenuation	1 - 3 dB
Rejection	30dB minimum

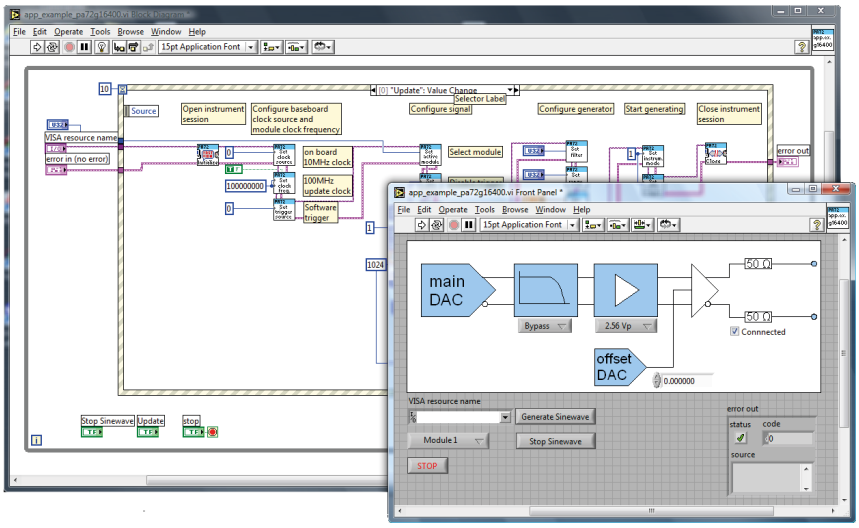


Custom 3e order band pass elliptic 20MHz

Software

The PA72 comes with a VXIplug&play compatible LabWindows/CVI driver, and a LabView driver. The driver API is fully documented, and gives you full control over the hardware. A LabView Application Example is included in the driver.

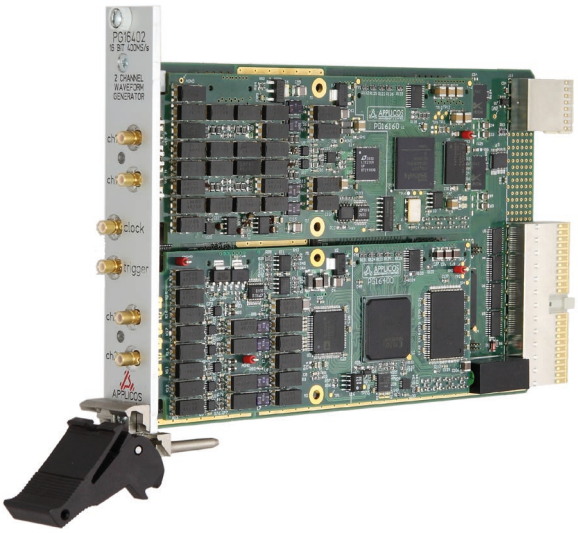
A Soft Front Panel tool is also included, which is a convenient way to quickly set-up the hardware of your module and start a measurement.



Ordering information

The order number consists of the code for the PA72 board and the codes for the upper (n) and lower (m) daughter boards:

Main board	+	Upper board	+	Lower board
PA72		0 = empty		0 = empty
PA72e		1 = PA72G16400		1 = PA72G16400
		2 = PA72G14180		2 = PA72G14180
		5 = PA72D16180A		5 = PA72D16180A
		6 = PA72D14130		6 = PA72D14130
		9 = PA72DIOS6016		9 = PA72DIOS6016
		F = PA72BPF*		F = PA72BPF*



* Filter daughter board (specify filter requirements separately)

Examples:

PA72-15 PA72 base board with PXI-1 bus interface
and a PA72G16400 generator on position 1 and a PA72D16180A digitizer on position 2

PA72e-20 PA72e base board with PXI-Express bus interface
and a PA72G14180 generator on position 1 and no board on position 2