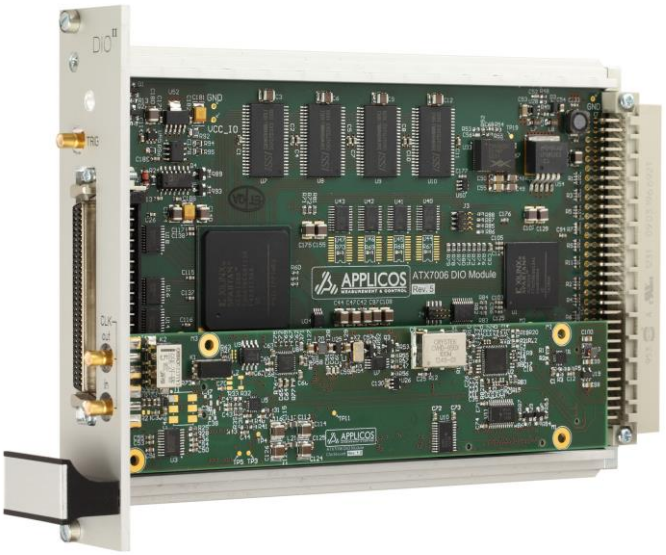
DIO^{-II}, Multimode Digital Source/Capture

DIO^{-II}

- Multimode Digital Source/Capture module
- Very low jitter clock generation
- Up to 50MHz data rate in low speed mode
- Up to 200MHz data rate in high speed mode
- Up to 1GHz clock rate via front clock out
- 20-bit parallel / 24-bit serial capture capability
- 64k x 16 pattern generator (low speed mode)
- Programmable clock delays (high speed mode)
- Programmable IO levels
- Exclusively for ATX series hardware platform



The DIO^{-II} module is a multimode digital source and capture unit. In Low Speed Mode it provides a 20-bit parallel or 24-bit serial I/O capability running at speeds up to 50MHz. In High Speed Mode, the DIO^{-II} provides a 16-bit parallel I/O capability up to 200MHz.

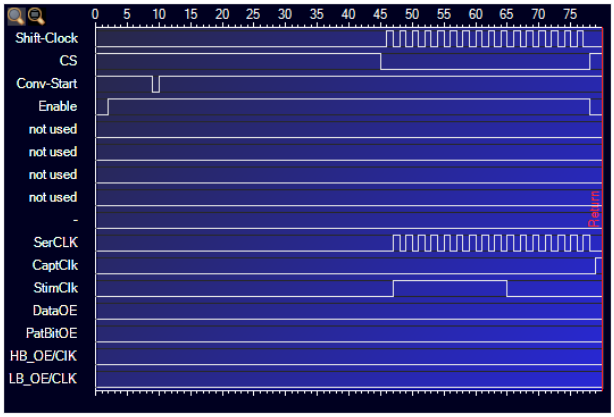
In both Modes, the Clock is generated by a low jitter PLL source that is capable of generating clocks from 320kHz up to 1GHz. In low speed mode the maximum usable clock frequency is 100MHz, in High Speed mode the maximum clock frequency via the backplane is 600MHz and via the front clock 1GHz.

The DO^{-II} supports external clocking (in or out), external trigger and frequency synchronization with an external reference source

The DIO^{-II} offers 8 Pattern Bits to the user for DUT synchronization and control. The remaining 8 Pattern Bits are used for control and synchronization of the analog source and capture modules through the ATX backplane..

This ensures coherent mixed-signal measurements thereby improving the accuracy of your measurement without need for "post-process" windowing.

The flexible pattern bit structure enables the implementation of various serial protocols as SPI, I^2C, I^2S, etc.

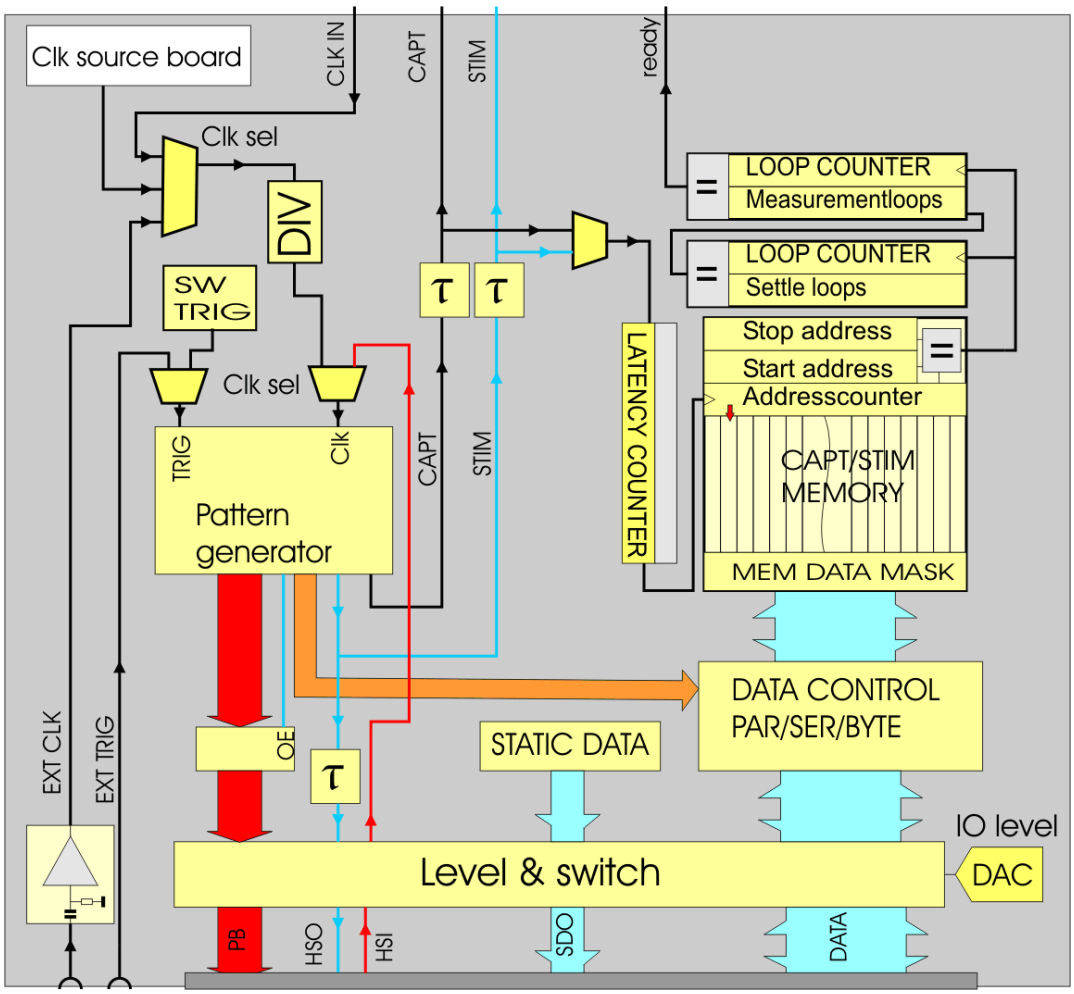


Example of pattern-bit programming

APPLICOS
MEASUREMENT & CONTROL

Multimode Digital Source/Capture

Block diagram (for low speed mode)



Specifications

Low Speed Mode

Pattern Generator	100MHz, 64kwords x 16-bits
Data I/O Pins / Bits	20-bit parallel / 24-bit serial
Data I/O Formats	parallel, byte-by-byte, serial
Source/Capture Depth	4M-words x 24-bits / 8M-words x 16
Internal clock frequency	320kHz to 100MHz
External clock frequency	DC to 100MHz
Data source/capture rate	DC to 50MHz
I/O Levels	Vil: 0.4V(max), Vih: 1.2V, 1.8-3.3V

High Speed Mode

Data I/O Pins	16-bit
Data I/O Formats	parallel
Source/Capture Depth	8M-words x 16-bits
Backplane clock frequency	320kHz to 600MHz
Data source/capture rate	DC to 200MHz
I/O Levels	LVDS

Separate Stimulus clock, Capture clock and DUT clock
All derived from the same low jitter main clock

Front panel Clocks

Clock output level (typical)	: 1.5Vpp / 50Ω
Clock output frequency	: 320kHz - 1GHz
Clock input Low Speed mode	: DC - 100MHz
Clock input High Speed mode	: 1MHz - 400MHz (ref. clock in)
Clock input threshold / imp.	: 0V or 1V (programmable) / 50Ω

General

Clock jitter (typical@100MHz)	: 190fs
Independent delay per clock	: 0-32ns (~0.5ns resolution)
Trigger input threshold level	: 1V (1kΩ)
Pattern bit trigger capability	: DC - 5MHz

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