

# Technical Innovation

## Maintaining IDDQ Measurement Accuracy in High Density Applications

“With increasing degrees of multi-site testing, the cost of power supplies will increase. Especially if reduced pin-count techniques are deployed, the power cost per site may dominate the channel cost per site. The cost increase in power supplies may be contained by innovations in power supply and power delivery technology.” [International Technology Roadmap for Semiconductors, 2009.]

Salland develops high performance device power supply (DPS) solutions for extreme high parallel testing. In doing so, our users can extend the capabilities of their standard ATE systems in a cost-effective approach. The ITRS roadmap of 2009 predicts that parallel testing for up to 2048 sites will be required. Salland has a working solution to add 640 individual DPS to existing test systems like the J750 from Teradyne. In developing this capability, we had to overcome a major challenge.

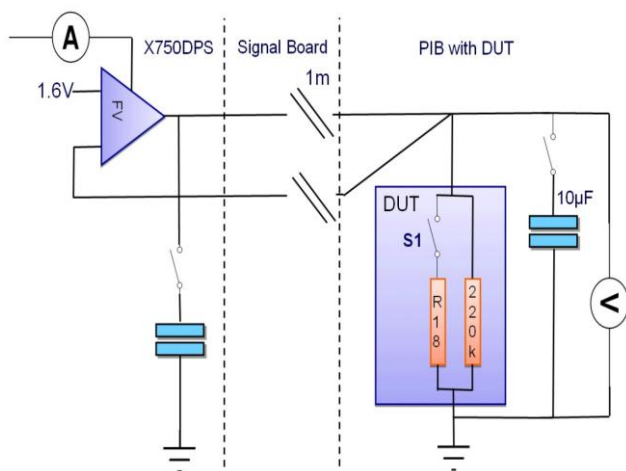


Figure 1. Simplified DUT Model

Due to shrinking voltages the voltage accuracy of the DPS must be high at higher currents and requires Force line sensing and Ground line sensing. One of the main challenges is the measurement of IDDQ. For normal high current operation the DUT requires a bulk capacitor to keep the voltage stable during large changes in load. However, IDDQ currents are small and can't be measured when the big bulk capacitor is still connected at the DUT. To illustrate this effect Salland created a simplified DUT model as shown in the diagram in Figure 1.

When the DUT switch “S1” is applied in order to simulate some typical IDDQ measurement current values, the current changes by a factor of 12X. Without a big bulk capacitor the current can be measured but the dynamic load regulation of a regular DPS is so slow that the resultant voltage at the DUT shows drops and spikes without a bulk capacitor.

Therefore, we need a bulk capacitor to get acceptable voltages at the DUT. However this makes current measurements especially at low values nearly impossible. The diagrams below shows the resultant current when a big bulk capacitor is connected - the larger the bulk capacitor the greater the error.

As shown in Figure 2: The current drops from 90mA to 7uA when the switch is applied. Thanks to an added bulk capacitor of 10uF, the voltage increase is limited to 50mV which is acceptable to many DUT's. But the current monitor line is out of scale and is not usable to

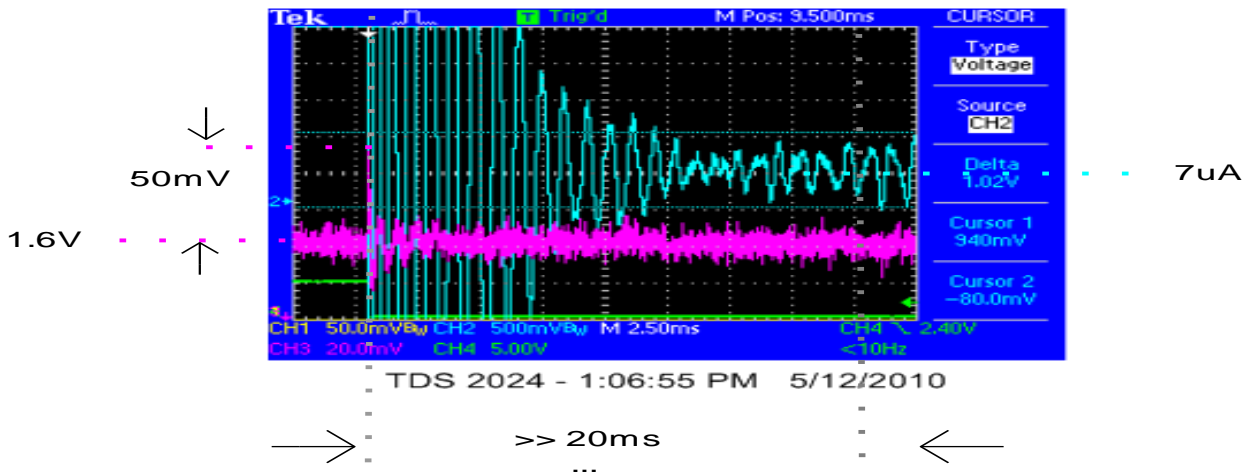


Figure 2. Current Response to Switch Applied.

measure the current. We would have to wait 20ms and perform some averaging to have any useful measurements.

An obvious solution is to switch off the bulk capacitor during IDDQ measurements. However this requires switch (relays) that consume valuable loadboard real estate. While this approach may be practical up to 32 sites, it becomes impossible at 256 sites and higher.

Salland solved this bulk capacitor challenge in our latest DPS product by moving all the required electronics to the instrument board and thereby simplifying the loadboard design. The simplification results in a trace-only design approach which by itself minimizes the persistent challenge of loadboard PCB routing with high site counts.

Typically IDDQ measurements are done multiple times at different settings of the DUT. Several hundred IDDQ tests are common practice. At high site counts with a lot of mathematical averaging this creates large volumes of data. Existing DPS instruments require the tester CPU to process this data. IDDQ test times become a critical factor. Salland's DPS solutions use state of the art interface standards to achieve a fast data transfer. The instrument board by itself can autonomously execute the complete IDDQ

measurements including averaging, capacitance switching and limit checking. The Salland instrument board executes the IDDQ measurements in full parallel with efficiency approaching the theoretical 100% even at sites counts > 512.

Salland continues to explore additional improvements of achieving accurate IDDQ measurements in high parallel applications. Possibilities include specialized IDDQ algorithms running directly on instrument hardware or even IDDQ measurement capabilities inside the DUT. Salland invites our readers to share their thoughts with us regarding these future techniques.

**Author: Rien Looijen** has more than 25 years of experience in semiconductor testing. He has been with Salland Engineering since 1992 where he worked on efficiency improvements of existing ATE ranging from add-on networking to CPU replacement projects. His main focus is research and productizing of ATE instruments with emphasis on high density DC instruments.

**Editor's Note:** If you are interested in the product referenced in this article that allows you to add up to 640 additional device power supplies to your J750,s, contact us and ask about the X750.